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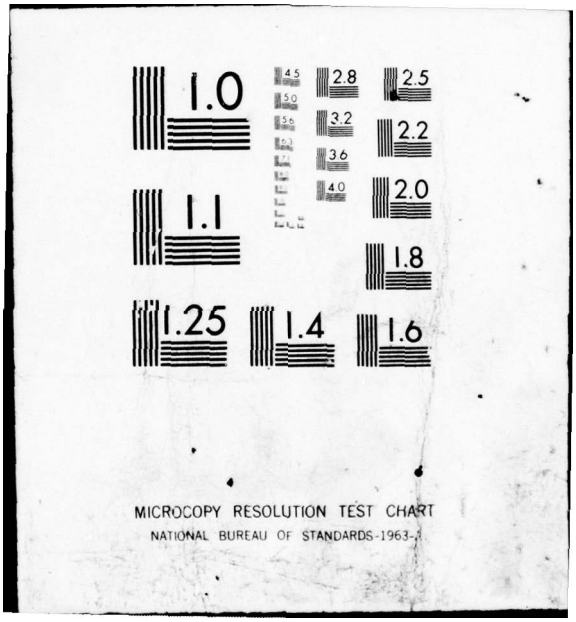
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Research and Development Technical Report
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PHOTOLITHOGRAPHIC TECHNIQUES FOR SURFACE ACOUSTIC WAVE (SAW) DEVICE

A. W. DOZIER

GROUND SYSTEMS GROUP
HUGHES AIRCRAFT COMPANY
FULLERTON, CALIFORNIA 92634

July 1975 to December 1978

Final Report: Volume 3 – Technical and Operational Par

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REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

(18) (19) 1. REPORT NUMBER: DELET-TR-75-0044-F-V-3

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

Pt not necessary as now given on Vols (e.g. Pt 1 + 2 in Vol 2

(6) 4. TITLE (and Subtitle): Photolithographic Techniques for Surface Acoustic Wave (SAW) Devices. [redacted] Volume 3, Technical and Operational, Part 3.

5. TYPE OF REPORT & PERIOD COVERED: Final – 1 July '75 to 31 December '78

6. PERFORMING ORG. REPORT NUMBER: (14) FR-79-12-40-VOL-3

7. AUTHOR(s): (10) A. W. Dozier

8. CONTRACT OR GRANT NUMBER(s): (15) DAAB07-75-C-0044

9. PERFORMING ORGANIZATION NAME AND ADDRESS: Hughes Aircraft Company, Ground Systems Group, Fullerton, California 92634

172 370

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62705A

11. CONTROLLING OFFICE NAME AND ADDRESS: Electronics Technology and Devices Laboratory (DELET-MM) USAERADCOM, Fort Monmouth, New Jersey 07703

12. REPORT DATE: Dec [redacted] 1978

13. NUMBER OF PAGES: (12) 100 p.

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)

15. SECURITY CLASS. (of this report): Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release, distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Surface Acoustic Wave Devices
Bandpass Filters
Tapped Delay Line Filters
Pulse Compression Filters
SAW Processing
SAW Packaging

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The object of the program was the establishment of a production capability for surface acoustic wave devices of varied design and material for the purpose of meeting estimated military needs for a period of two years after the completion of the contract, and to establish a base and plans which may be used to meet expanded requirements. The primary requirement was the pilot line production of devices that are reliable, reproducible, and low cost.

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The first phase of this program required the design, fabrication and testing of a total of 60 prototype bandpass, tapped delay line and pulse compression SAW filters on both lithium niobate and ST-quartz. The First Engineering Phase (Phase I) electrical testing demonstrated that the device designs generally met the specifications imposed by the program. Deviations from specification, which required additional test to optimize the levels of padding and/or shunt resistance and capacitance, were resolved during the Second Engineering Phase (Phase II) for the PC-Q, PC-LN and TDL-200. Deviations from the insertion loss specification occurred with the BP-LN and TDL-100 designs. In the former case, a redesign excluding the program-specified multi-strip coupler, was theoretically evaluated. In the latter case, as pointed out in the Hughes proposal, a theoretical analysis precluded the possibility of a specification accommodation. It was necessary to revise the specification for both designs since the customer insisted on utilization of the multistrip coupler in the BP-LN.

Testing of modified semiconductor pin packages during Phase II demonstrated these to be suitable, cost-effective replacements for the machined chassis employed for Phase I. A Quartz orientation problem was highlighted in Phase I and negotiated during Phase II. The quartz vendor implemented an effective screening procedure for the off-orientation problem. However, problems with this vendor continued in the form of substrate surface defects. Other major yield problems encountered during these portions of the program resulted from the dicing and mask making operations. The Phase I and Phase II efforts resulted in a finalized layout, electrical specifications and test procedure for the Third Engineering Phase (Phase III).

Phase III involved fabrication of a larger quantity (50 ea.) of confirmatory devices which were sampled at a high rate and subjected to rigorous life and environmental testing. Phase III was successfully completed with delivery and acceptance of the confirmatory samples. The device configuration is detailed as it existed for Phase III along with assembly details, results and conclusions from the Confirmatory Sample production run (Phase III).

The Fourth Engineering Phase (Phase IV) of the program was pilot line production effort of 150 each of the devices scheduled to be delivered. Solder scaling was identified as a problem area during Phase IV for SAW devices in Phase III packages. New solder seal screening and processing procedures were investigated. In addition, alternative sealing approaches were evaluated. These procedures, Tungsten Inert Gas (TIG) and projection and seam welding were demonstrated to be more compatible with SAW processing. They are especially suitable for high volume production.

Phase IV pilot line production was completed with the delivery of approximately 150 of each of the device types. Some devices were shipped short due to the inability to locate a second source for projection welding, and the extended lead time in reprocurement of packages capable of being sealed by alternate procedures.

Data from Phases I through IV are presented in the Technical and Operational volume of the Final Report. Pilot Line process flow and related documentation are presented in the Process Specification Volume of the Final Report. All inspection positions, and quality control procedures for Phase IV are presented in the Quality Control Volume of the Final Report. Cost analysis and labor distribution for all facets of the program are covered in a non-distributable volume of the final report.

The program will include preparation of a General Report, which will consist of an analysis of equipment and facilities required to produce SAW devices of the type produced in the Pilot Run at a rate of 500 per month. In addition, an Industry Demonstration was prepared which verbally and visually presented all facets of the MMT program through the Pilot Run.

CONTENTS OF VOLUME 2, PARTS 1 AND 2

CONTENTS OF VOLUME 3, PART 3

APPENDICES FOR VOLUME 2, PARTS 1 AND 2

APPENDICES FOR VOLUME 2, PARTS 1 AND 2 (Continued)

APPENDICES FOR VOLUME 3, PART 3

LIST OF FIGURES FOR VOLUME 2, PARTS 1 AND 2

LIST OF FIGURES FOR VOLUME 2, PARTS 1 AND 2 (Continued)

LIST OF FIGURES FOR VOLUME 2, PARTS 1 AND 2 (Continued)

LIST OF FIGURES FOR VOLUME 3, PART 3

LIST OF TABLES FOR VOLUME 2, PARTS 1 AND 2

LIST OF TABLES FOR VOLUME 3, PART 3

PURPOSE

This report presents the results of the three year effort in satisfying the requirements of a Manufacturing Methods and Technology Program devoted to a representative range of surface acoustic wave (SAW) device designs.

The objective of this program was to establish a production capability for the purpose of meeting estimated military needs for a period of two years after the completion of the contract, and to establish a base and plans which may be used to meet expanded requirements. The manufacturing method emphasized the photolithographic fabrication of SAW devices that are reliable and reprodicible at low cost.

Specific tasks included establishing and demonstrating a capability to manufacture the six SAW device designs on a pilot line basis using methods and processes suitable for a production rate of 150 devices per month for each type. In addition, engineering analysis and planning remains to be accomplished for expansion of the manufacturing capability which could accommodate the production of such devices at a rate of 500 each per month. This analysis and planning will be delivered in the General Report.

The program was divided into four phases. The first (Phase I First Engineering Sample) addressed the design, fabrication and analytical testing of six prototype SAW devices that are representative of the major current and potential application of the technology. While these device requirements did not represent the state-of-the-art in an R & D sense, they were of such complexity as to require a serious design effort in each case.

The second phase (Phase II – Second Engineering Samples) was performed to redesign those devices that failed the intended design specification. The net result of this effort was to be functional electrical specification adherence, based on a cost effective packaging commitment.

The third phase (Phase III – Confirmatory Samples) was to test and conform to specification for both the electrical and environmental commitment of the various devices. The final phase (Phase IV – Pilot Run) was to test the reproducibility of those predetermined electrical and environmental requirements in a high volume (500 per month) production environment. A key result of this phase was the establishment of meaningful manufacturing cost data on each device as well as a comparison of this data to the prior low volume efforts of the earlier phases. These data will then be extrapolated to a production rate of 500 per month with assumptions regarding facilities and equipment in the General Report.

GLOSSARY

SAW	–	Surface Acoustic Wave
BP-Q	–	Bandpass Filter – ST Quartz Substrate
BP-LN	–	Bandpass Filter – Lithium Niobate Substrate
TDL-100	–	Tapped Delay Line Filter – 100 MHz – ST Quartz Substrate
TDL-200	–	Tapped Delay Line – 200 MHz – ST Quartz Substrate
PC-Q	–	Pulse Compression Filter – ST Quartz Substrate
PE-Q	–	Pules Expansion Filter – ST Quartz Substrate
PC-LN	–	Pulse Compression Filter – Lithium Niobate Substrate
PE-LN	–	Pulse Expansion Filter – Lithium Niobate Substrate
ST	–	Quartz orientation, ST cut (42^{o} 45'), X propagating
YZ	–	Lithium Niobate orientation, Y cut Z propagating
TIG	–	Tungsten Inert Gas Welding
MSC	–	Multistrip Coupler
K^2	–	Electromechanical Coupling Constant
f_o	–	Center frequency
B	–	Bandwidth
T	–	Time Delay
TXB	–	Time Bandwidth Product
VSWR	–	Voltage Standing Wave Ratio
DUT	–	Device Under Test
L_{INS}	–	Insertion Loss
$S_{S.L.}$	–	Sidelobe Suppression
$S_{f.t.}$	–	Feedthrough Suppression
S_{Spur}	–	Spurious Suppression
TTS	–	Triple Transit Signal

3.0.0
SAW DEVICE REDESIGN – SECOND ENGINEERING SAMPLES (PHASE II)

3.0.0 SAW DEVICE REDESIGN – SECOND ENGINEERING SAMPLE (PHASE II)

Phase II of this program was to accomplish reiteration of the Phase I design to meet the original electrical specification. In some cases the specified parameter could not be met, and was respecified accordingly prior to initiation of Phase II. The first segment of this section will address electrical measurement techniques and equipment utilized for Phases I and II. This will be followed by a discussion of deviations from the original electrical specification (Appendix I, Volume 2 of the Final Report) and redesign approaches. Final specification accommodations will then be discussed.

During Phase II, a dedicated (balanced) production line was set up to accommodate the 150 devices per month production rate requirements of Phase IV, the Pilot Run. In preparation for the production rate, hermeticity, and dimensional requirements of Phase III (Confirmatory Sample Fabrication-50 each part type) and Phase IV (Pilot Run-150 each part type), semiconductor package types were utilized, and chrome masks were restepped on array sizes compatible with the requirements of the specification (Appendix I, Volume 2 of the Final Report). Electrical implications of the new packaging format will be discussed in the section on redesign of Phase I devices, along with mask changes which impacted the electrical performance of the devices. Other considerations related to processing of the devices will be covered in a section on processing aspects of device fabrication.

3.1.0 ELECTRICAL TEST PROCEDURES AND TYPICAL DATA FOR PHASES I AND II

Electrical tests of the SAW Devices fabricated during Phases I and II of this program were performed in the R and D Laboratory. As a result, equipment and procedures were slightly different from those used in Phases III and IV (the Confirmatory Sample and Pilot Run phases), which used a dedicated test area. Test procedures and equipment used in Phases I and II can be seen in Appendix VII. Procedures and equipment used for the Confirmatory Sample (Phase III) and Pilot Run (Phase IV) phases were those detailed in the test specification of the Process Specification Volume (Dwg. No. 1950512-800, Volume I of the Final Report). It should be noted that both of these documents were used as training aids and are somewhat tutorial in nature. Plots of typical raw data for all measurement techniques and all device types can be seen in Appendix VIII. Phase I specimens utilized SMA type connectors, and slotted aluminum package assemblies. Phase II devices were packaged in standard hybrid packages, requiring the use of test fixtures which will be described in a subsequent section. Tuning procedures are essentially the same as those used for Phases III and IV and are included in Appendix VII for reference.

3.2.0 SPECIFICATION DEVIATIONS AND RECOMMENDED CHANGES

Section 2.0.0 covered the initial design (Phase I) of the six device types required under this contract. At the conclusion of Phase I, it was noted that certain parameters of the devices built for Phase I were either marginal or exceeded specified values as required in Appendix I Volume 2 of the Final Report. A summary of these deviations and marginal parameters can be seen in Table 3.2.1. Further analysis and testing was performed prior to initiation of the Phase II build, with the conclusion that certain specification modifications were required. A summary of these recommended specification revisions can be seen in Table 3.2.2. Prior to initiation of Phase II device fabrication, the specification was modified to incorporate Table 3.2.2 and the Errata sheet of Appendix I, Volume II of the Final Report. This modified specification can be seen in Appendix IX. All areas deviating from the original specification (Appendix I, Volume 2) are highlighted in the margin. A summary of the revised specification electrical parameters from Appendix IX can be seen in Table 3.2.3. [It should be noted that this modification of the original specification was erroneously substituted with an earlier modification in the Process Specification Volume. Appendix IX was the modified version used for Phases II, III and IV of this Program.] Recommendations and rationale based on engineering analysis for the modification of this specification are outlined below by individual device type. In light of the specification changes, certain resistance and toroid changes were made to optimize insertion loss. Final changes to device design prior to Phase II fabrication will be discussed at the conclusion of this section.

3.2.1 Linear Phase Bandpass Filter-Quartz Substrate (BP-Q)

The insertion loss achieved on Phase I devices was marginally at 22 dB, potentially lowering device yield. In order to lower this value to an acceptable 20 dB, the series resistance on both input and output transducers was reduced. This raised the VSWR level marginally in excess of the specification, requiring a specification modification to 2:1.

The impact of the marginal VSWR level was expected to lower the production yield of this device by as much as twenty-five percent. This, in turn would raise the estimated manufacturing cost of the SAW dice ($8.51) by forty-five percent ($12 38). Since, however, marginal VSWR would not be identified until final test, additional labor would be incurred for package rework and test. Combined with the increased die cost, this would raise the manufacturing cost of the final SAW device to $30.76 compared to an estimated proposal cost of $24.72.

3.2.2 Linear Phase Bandpass Filter-Lithium Niobate Substrate (BP-LN)

During Phase I of the program, Hughes learned that the multistrip coupler (MSC) specified for this device was incurring additional insertion loss (see Section 2.2.1 of Volume 2 of the Final Report). The alternative of eliminating the MSC was examined, whereby a theoretical evaluation of a number of designs was then performed. Of the best of these, it was found that the inherent Q of the transducers caused the theoretical insertion loss (15 dB) and spurious echo suppression (35 dB) to barely be met. Adaptation of this design required a relaxed spurious echo suppression of 30 dB. A more serious problem was the required addition of six lumped matching network components in the new

TABLE 3.2.1. SUMMARY OF AVERAGES OF ELECTRICAL DATA FROM PHASE I WHICH DEVIATED FROM THE ORIGINAL SPECIFICATION

Device	Para. SCS 476	Average Measured Parameter	Remarks
1. BPQ	3.10.5.2a	Insertion Loss = 22 dB	Very marginal – SCS 476 I. L. = 22 ± 2 dB
	3.10.9	VSWR < 1.2:1	Marginal with respect to < 1.5:1 in SCS 476
2. BP-LN	3.10.5.2b	Insertion Loss = 21 dB	Out of spec. SCS 476 I. L. = 15 ± 1.5 dB
	3.10.9	VSWR < 2.3:1 dB	Out of spec. SCS 476 < 1.5:1
3. TDL-100	3.10.5.3a	Insertion Loss = 40 dB	Out of spec. SCS 476 = 30 ± 3 dB
	3.10.8	Spurious Supp. = 28 dB	Out of spec SCS 476 > 35 dB
	3.10.9	VSWR < 6:1	Out of spec. SCS 476 < 1.5:1
4. TDL-200	3.10.5.3b	Insertion Loss = 38 dB	Out of spec. SCS 476 = 30 ± 3 dB
	3.10.6.3b	Sidelobe Supp. 16 to 19 dB	Marginally out of spec. SCS 476 ≥ 19
	3.10.7	Feedthrough Supp. = 50 dB	Marginally in spec.
	3.10.9	VSWR ≤ 3.5:1	Out of spec. SCS 476 ≤ 1.5:1
5. PC-Q	3.10.5.1a	Insertion Loss 39 to 48 dB	Better than spec SCS 476 = 55 ± 5
	3.10.6.1a	Sidelobe Supp. 19 to 28 dB	Marginally out of spec. ≥ 25 dB
	3.10.9	VSWR = 2:1	Out of spec. SCS 476 < 1.5:1
6. PC-LN	3.10.5.1b	Insertion Loss 24 to 28 dB	Better than spec. SCS 476 = 30 ± 3 dB
	3.10.6.1b	Sidelobe Supp. 19 to 28 dB	Marginally out of spec. ≥ 25 dB
	3.10.9	VSWR > 10:1	Out of spec. SCS 476 < 1.5:1

TABLE 3.2.2. SUMMARY OF SPECIFICATION (SCS 476) CHANGES FOR PHASE II

Device	SCS 476 Paragraph	Parameter	Old Value	New Value
1. BP-Q	3.10.9.2a	VSWR	≤ 1.5:1	≤ 2:1
2. BP-LN	3.10.5.2b	Insertion Loss (dB)	= 15 ± 1.5	= 20 ± 1.5
	3.10.9.2b	VSWR	≤ 1.5:1	≤ 3:1
3. TDL-100	3.2.1	Metallization Thickness (Å)	1000-2000	300-2000
	3.10.5.3a	Insertion Loss (dB)	30 ± 3	27 ± 3
	3.10.6.3a	Sidelobe Supp. (dB)	≥ 19	≥ 17
	3.10.9.3a	VSWR	≤ 1.5:1	≤ 4:1
4. TDL-200	3.2.1	Metallization Thickness (Å)	Same as TDL-100	
	3.10.5.3b	Insertion Loss (dB)	30 ± 3	26 ± 3
	3.10.6.3b	Sidelobe Supp. (dB)	Same as TDL-100	
	3.10.9.3b	VSWR	≤ 1.5:1	≤ 3:1
5. PC-Q	3.10.5.1a	Insertion Loss (dB)	55 ± 5	50 ± 5
	3.10.9.1a	VSWR	≤ 1.5:1	≤ 2.5:1
6. PC-LN	3.10.6.1b	Sidelobe Supp. (dB)	> 25	>20 first leading and trailing >25 all others
	3.10.9.1b	VSWR	≤ 1.5:1	≤ 3.5:1

TABLE 3.2.3. SUMMARY ELECTRICAL TEST MATRIX FOR APPENDIX IX

Device	f_o (MHz)	$B_{3\ dB}$ (MHz)	τ (μS)	τXB[1]	L_{INS} (dB)	S_{SL} (dB)	S_{ft} (dB)	S_{spur} (dB)	VSWR
BP-Q	98-102	1.96-2.09	2.0 ± 0.02	4:1	18-22	≥ 35	≥ 50	≥ 35	≤ 2:1
BP-LN	147-153	29.4-30.6	2.0 ± 0.01	60:1	18.5-21.5	≥ 35	≥ 50	≥ 35	≤ 3:1
TDL-100	98-102	10 ± 0.2 (1)	12.7 ± 0.01	127:1	24-30	≥ 17	≥ 50	≥ 35	≤ 4:1
TDL-200	196-204	10 ± 0.2 (1)	12.7 ± 0.01	127:1	23-29	≥ 17	≥ 50	≥ 35	≤ 3:1
PC-Q	147-153	50 ± 1 (2)	2.0 ± 0.01	100:1	45-55	≥ 25	≥ 50	≥ 35	≤ 2.5:1
PC-LN	147-153	50 ± 1 (2)	2.0 ± 0.01	100:1	27.33	≥ 20 ≥ 25	≥ 50	≥ 35	≤ 3.5:1

Notes:

[1]This is the chip rate of the biphase-coded waveforms to which the respective biphase-coded tapped delay line filters are to be matched.

[2]This is the difference between the maximum and minimum instantaneous frequencies of the unweighted linear FM waveform to which the characteristics of the respective linear FM pulse compression filters are to be matched.

design, including two broadband impedance transformers. The manufacturing cost of the additional components was estimated to be $9.91, compared to a SAW Die cost of $8.51. Furthermore, it was noted that this design had not been evaluated experimentally, and actual performance data could deviate from theoretically calculated values due to deviations from ideal performance of the lumped matching network components. As a result of these considerations, the original design was retained with the MSC, and the specification was relaxed to meet the performance demonstrated in Phase I.

3.2.3 Biphase-Coded Tapped Delay Lines-Quartz Substrate, 100 and 200 MHz Center Frequency (TDL 100 and TDL 200)

A VSWR of 1.5:1 could not be achieved on the TDL-100 with an insertion loss of 30 dB under any circumstances. A somewhat reduced VSWR could be obtained with the addition of two additional components on the input transducer and one on the output tap array at the expense of insertion loss. The specified metallization thickness causes the spurious echo suppression specification to be exceeded. The specified sidelobe suppression level was only marginally achieved during Phase I (15 to 18 dB vs specification of 19 dB) and would also be improved by metallization thickness reduction.

Addition of the extra components on the input and output transducers to improve VSWR would cause a significant system parameter (insertion loss) to be sacrificed for a relatively insignificant parameter, VSWR. (See Appendix V, Volume II of the Final Report). The additional component manufacturing cost to lower VSWR was estimated at $3.46, compared to a SAW die cost of $10.05. The marginal value of VSWR achieved would also impact production yields in an adverse manner during the Phase III and IV portions of the program similar to the BP-Q. Additionally, the metallization thickness requirement in the original specification (1000Å to 2000Å) would result in zero device yields due to spurious echo suppression. As a result, the metallization thickness and VSWR requirement were relaxed from the original specified value, and the sidelobe suppression and insertion loss requirements were improved from the original. The same rationale as developed for the TDL-100 applied to the TDL-200. However, since the fractional bandwidth of the device was smaller, the suggested VSWR was lower.

3.2.4 Linear-FM Pulse Compression Filter-Quartz Substrate (PC-Q)

A VSWR of 1.5:1 required the addition of a discrete resistor on the input side of the matching network. This would increase insertion loss and component cost. A significant system parameter (insertion loss) would again be sacrificed for a relatively insignificant (see Appendix V, Volume 2 of the Final Report) parameter, VSWR. The additional cost at the manufacturing level was estimated to be $1.01 to compare to a SAW die cost of $7.02. As a result, the VSWR specification was relaxed with a corresponding improvement in the insertion loss requirement.

3.2.5 Linear-FM Pulse Compression Filter-Lithium Niobate Substrate (PC-LN)

A lower VSWR would require the addition of at least two components. The sidelobe suppression limit was attributed to an improper matching between the transducer and the external circuit impedance. The identification and resolution of this anomally would require the implementation of a significant R&D program.

In regard to the VSWR, the additional components and labor were estimated to cost $4.96 per device compared to the SAW die cost of $6.71. As a result, the sidelobe suppression and VSWR specification were relaxed.

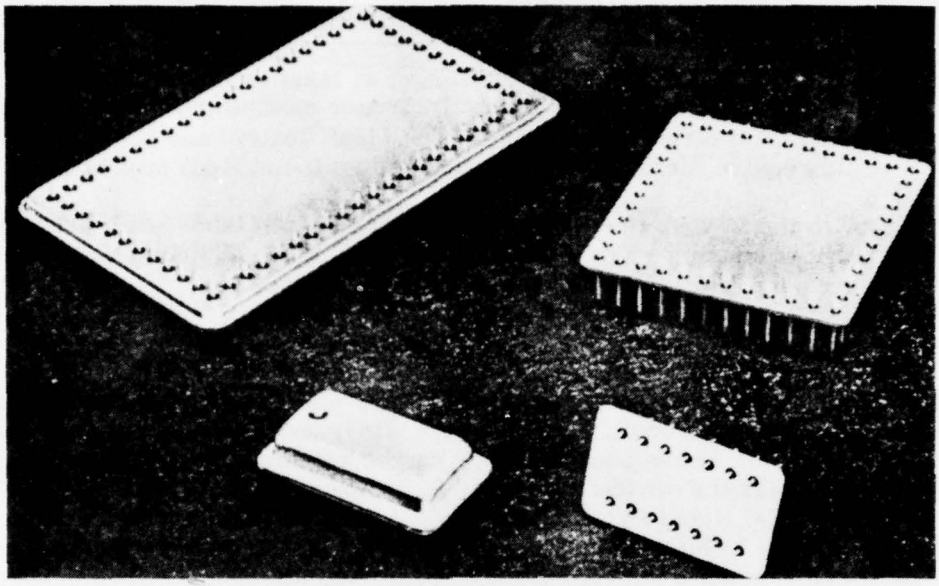
3.2.6 Implications of Phase II Design on Electrical Performance

As was mentioned previously, standard semiconductor pin packages were used on Phases II-IV to reduce device cost ($10 vs. $107) and effect hermeticity as required contractually. These package types can be seen in Figure 3.2.4. Candidate packages selected for the device types on this program were: P/N 20221 for BP-Q, BP-LN, PC-Q, PC-LN and P/N 20117* for TDL-100, TDL-200. Package covers, P/N 20216-159* and P/N 20118-175* respectively, were chosen with sufficient clearance to accommodate the toroid required for tuning. Solder sealing was chosen as a candidate sealing process for the program, which required tin plating on the package header. Gold wire bonding interconnection of the crystal required gold plating to be present on the pins. Device layouts utilizing these package types can be seen schematically in Figure 3.2-5. Note the excessively long wire bonds required to bond the far side of the crystal to the pins which are utilized as an interconnect between the crystal/toroids, and as ground lugs. These bonds are required as a result of the tin plating on, and excessive width of the header. This situation would have been avoided by the use of solderable and TC bondable substrates, but was not felt to be cost effective.

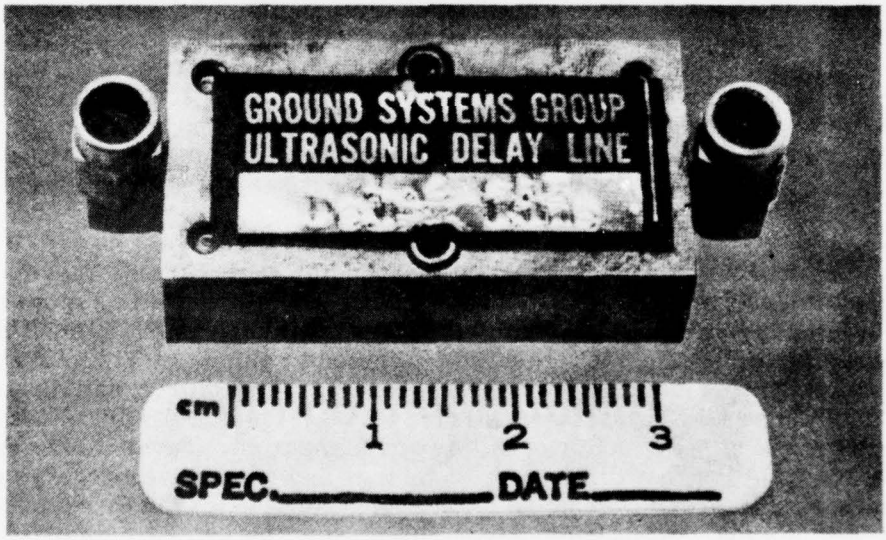
At the onset of Phase II, it was noted that feedthrough of the devices in semiconductor packages was degraded from that witnessed in Phase I in slotted aluminum assemblies utilizing SMA connectors. Several experiments utilizing shielding internal and external to the package were conducted to elucidate this problem without success. Initially, the test fixture was viewed as the culprit, with the modification of the fixture taken as shown in Figure 3.2.6. Upon preliminary testing of PC-Q devices, out of spec feedthrough was again apparent. Several internal septums were installed (beryllium copper spring, and conductive rubber) with an initial substantial improvement in device feedthrough, though the problem reoccurred during further testing. See Figure 3.2.7. [Note that the lobe at 2 microseconds in b) and c) was attributable to triple transit phenomena, and is not affected by packaging changes. Also, data in b) and c) was recorded using a different level of attenuation than in a)]. The final solution to the feedthrough problem was exhibited by utilization of the test fixture depicted in Figure 3.2.8.

It can be seen that the new test fixture firmly grounds the entire header through the use of chromeric gasket material, rather than effecting ground through the pins only. The tune operation was accomplished using a lid and top plate with

*Tekform Co., Anaheim, California



(a) TYPICAL SEMICONDUCTOR PIN PACKAGES



(b) MACHINED CHASSIS PACKAGE

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Figure 3.2-4. Comparison of First and Second Engineering Phase Packaging

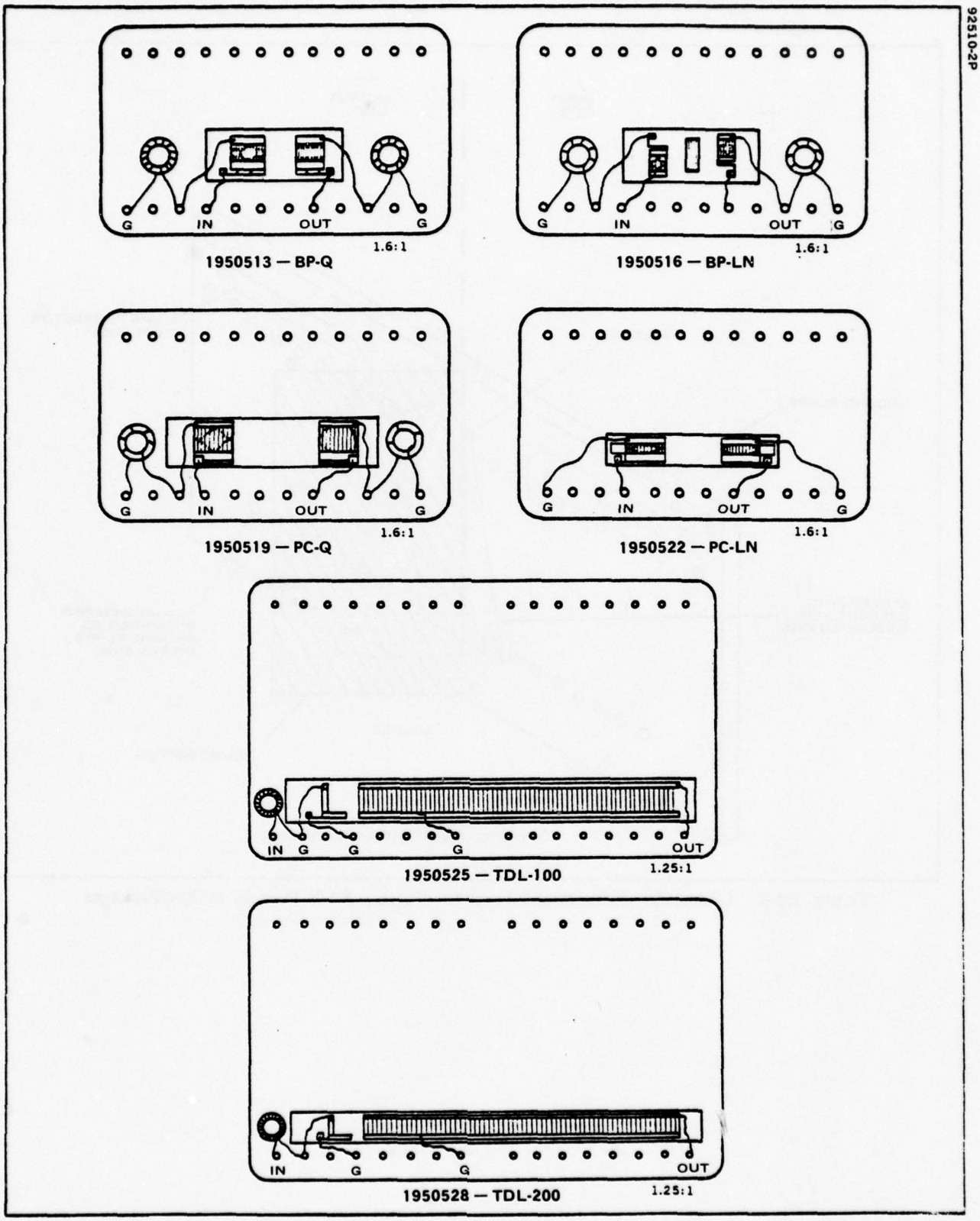


Figure 3.2-5. MMT SAW Device Configuration

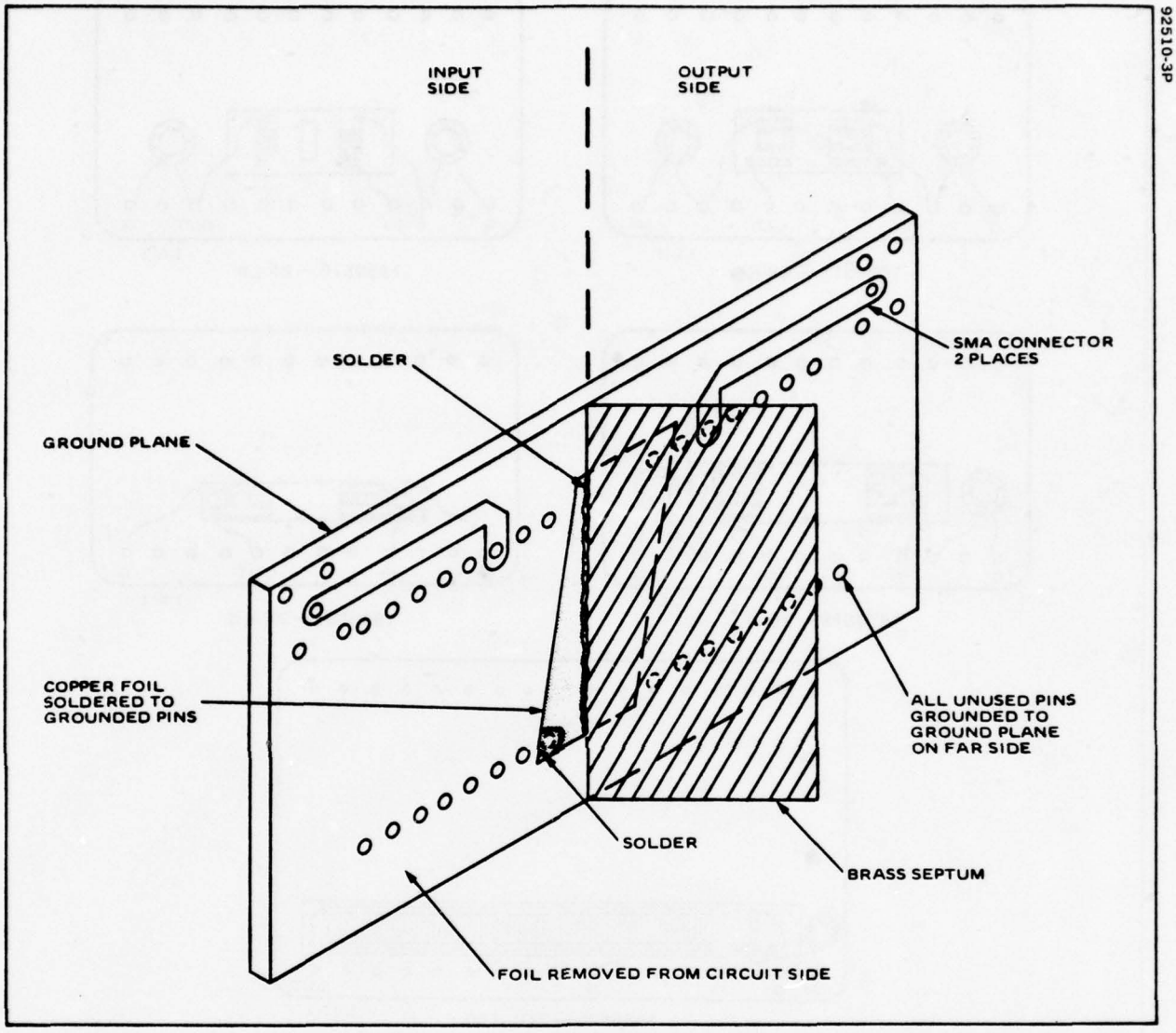


Figure 3.2-6. Underside of PC Board Used for Testing SAW Devices in Pin Packages

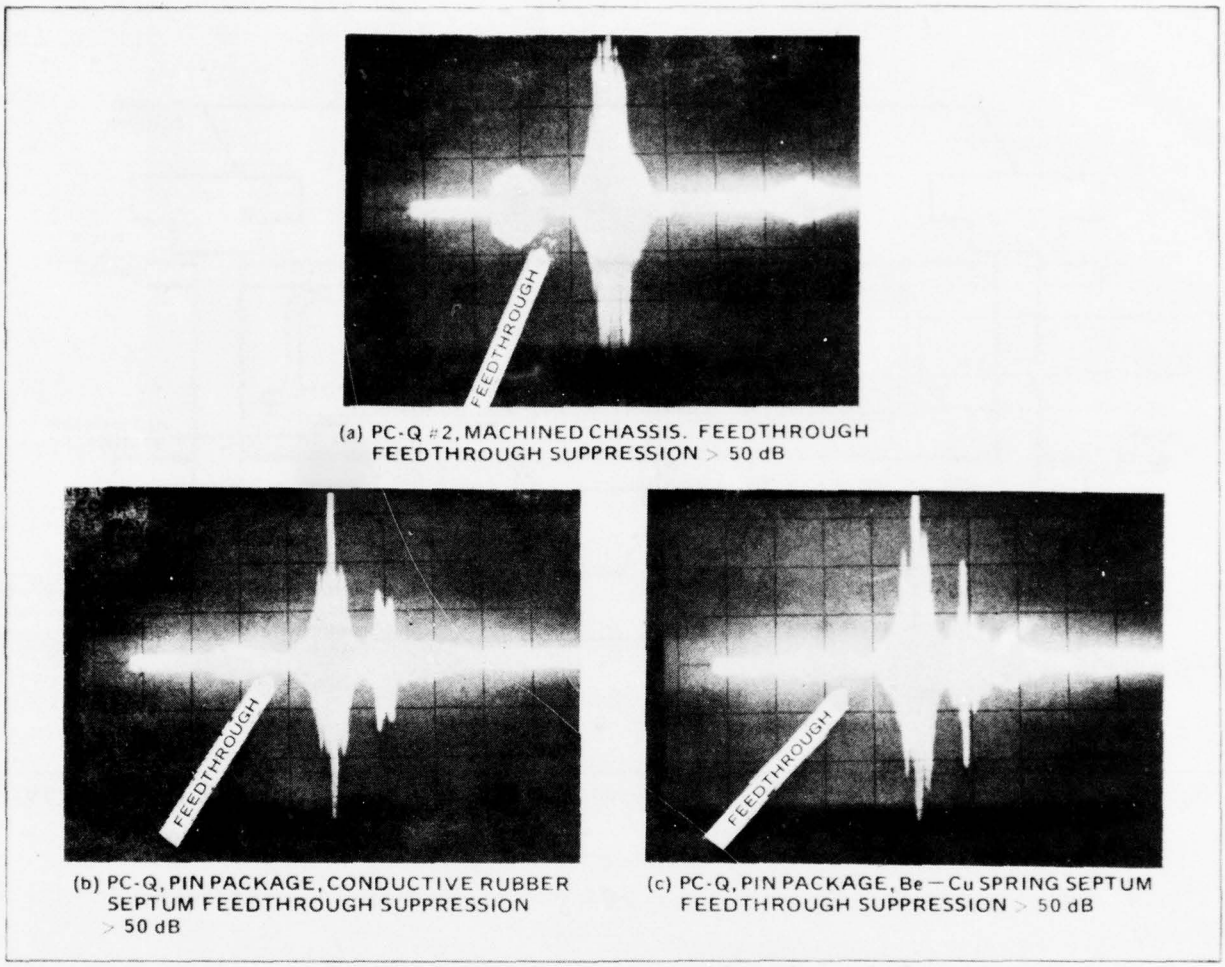


Figure 3.2-7. Recompressed Pulse of PC-Q Illustrating Feedthrough Levels for Various Packaging and Shielding Configurations. Vertical scale 50 mV/div. Horizontal scale 2 μS/div.

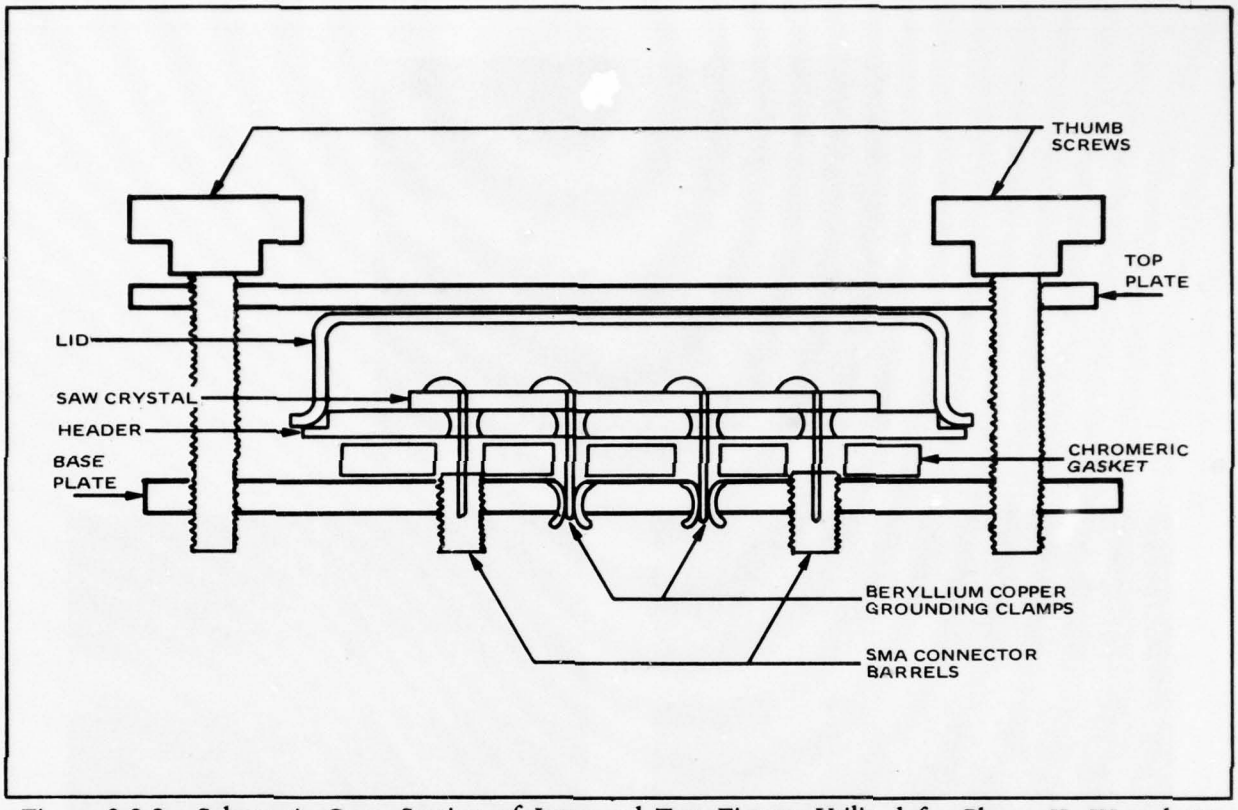


Figure 3.2.8. Schematic Cross Section of Improved Test Fixture Utilized for Phases II, III and IV

a hole allowing access to the toroids. It was determined during Phase II precap testing that feedthrough specifications could be met on all device types without the use of an internal septum. All devices were delivered for Phase II utilizing the above design improvements without the internal septum. Several additional design changes were instituted upon completion of Phase II to further optimize the feedthrough situation. These consisted of shorting the ground pins to the header on all designs, adding a ground pad between transducers on the TDL's, and deleting the long wire bonds running over the shunt resistors on the PC-LN design. The latter required addition of a moly tab, and was not used on the other designs due to the extra assembly steps required. In addition, it was noted that the dicing guides on the wafers were not entirely removed, leaving a continuous metal stripe running along the edge of the crystal. This was felt to be a possible contributor to excess feedthrough, and was subsequently corrected at the chrome mask level. The layout alterations can be seen in Figure 3.2.9.

3.3.0 PHASE II ELECTRICAL DATA

Phase II specimens were fabricated and assembled as shown in Figure 3.2.8, and tested per procedures outlined in Appendix VII. Electrical characteristics were required to be in conformance with Table 3.2.3. Since hermeticity was not required for Phase II, only precap data was collected. Lids were spot soldered in place prior to shipment to prevent handling damage. Although it has been noted that electrical characteristics change with lid installation for designs other than those used in this program, precap data was found to agree within measurement error with post lid installation data for these designs. Data for the specimens shipped in fullfillment of Phase II requirements (10 of each part type) can be seen in Table 3.3.1. It should be noted that bandwidth, B, was not measured for the TDL and PC devices. This parameter is determined by the transmitted signal and is described in Appendix VI, Volume II of the Final Report. Similarly, group delay, τ, was not measured for the PC devices. Time bandwidth product, $\tau X \beta$, is calculated only for the BP and TDL devices. As can be seen, there is little variation of these parameters (τ, β, and $\tau X \beta$) from those determined for the average value of Phase I samples. This is to be expected, since these parameters are set by the mask and crystal orientation. It should be noted that specimens denoted as "dashed", detuned, open, and broken bond wire in Table 3.3.1 are included for reference only and were repaired prior to shipment. Dashes are entered at data entries in Table 3.3.1 for speciments failing a previous test. Once a specimen failed a test, further testing was not performed. A blank entry in Table 3.3.1 indicates that no specimen with that serial number was fabricated.

A summary of the failure data can be seen in Table 3.3.2 expressed as a percentage of specimens tested passing the noted test. Corrective actions/failure analyses of failed parts can be seen in Table 3.3.3. Each box in the matrix will be discussed individually below by device type.

Quartz Linear Phase Bandpass Filter (BP-Q)

S/N #7 failed S_{sp} by 3 dB. Upon application of extra RTV on the end of the crystal, the part met specification.

S/N #6 failed the VSWR specification, but was retuned by adjusting the coils on the toroid. This failure was interpreted to be the result of excess RTV in in the center of the toroid core.

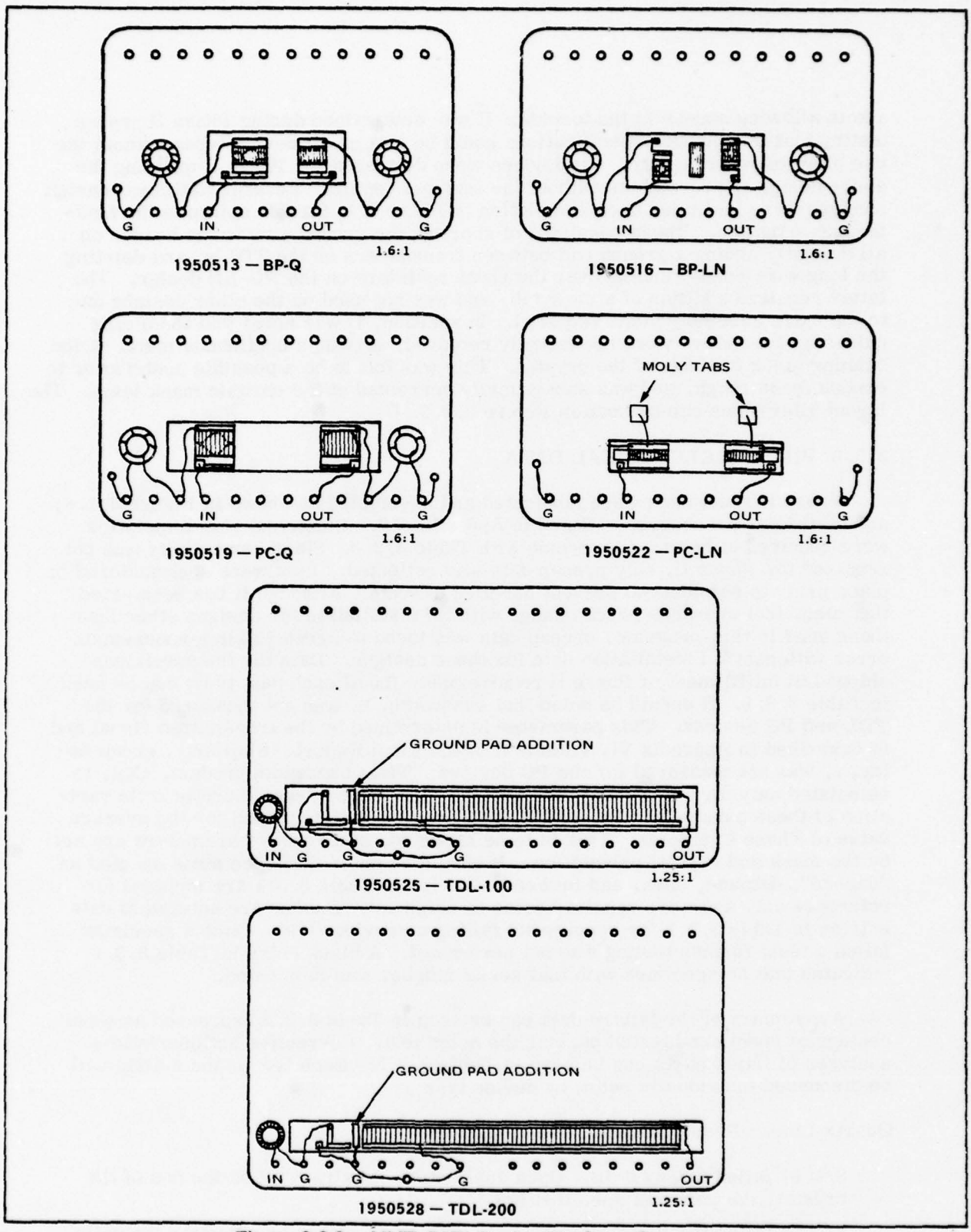


Figure 3.2.9. MMT SAW Device Final Configuration

TABLE 3.3.1. RAW DATA PHASE II SPECIMENS

Device Type	SCS-476	MEASURED DATA 1	2	3	4	5	6	7	8	9	10	11	12
					3.10.1 fo (MHz)								
BP-Q	100±2	100.25	100.25	100.25	100.25	100.25	100.25	100.25	100.25	100.25	Open		
BP-LN	150±3	150.5	150.5	150.5	150.5	150.5	150.5	150.5	150.5	150.5	150.5	150.5	
TDL-100	100±2	100.078	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
TDL-200	200±4	200	200	200	200	200	200	200	200	200	200	200	200
PC-Q	150±3	149.45	149.4	149.4	149.46	149.45	149.4	149.4	149.4	149.4	149.4		
PC-LN	150±3	150	150	150	150	150	150	150	150	150	150	150	150
					3.10.2 β (MHz)								
BP-Q	2±0.04	–	2.04	2.04	2.04	2.04	2.04	2.04	2.04	2.04			
BP-LN	30±0.6	30	30	30	30	30	30	30	30	30	30	30	
TDL-100	10±0.2												
TDL-200	10±0.2				Not Measured								
PC-Q	50±1												
PC-LN	50±1												
					3.10.3 τ (μsec)								
BP-Q	2±0.01	–	1.9771	1.9771	1.9771	1.9771	1.9771	1.9771	1.9771	1.9771	–		
BP-LN	2±0.01	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	
TDL-100	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7
TDL-200	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7	12.7
PC-Q	2±0.01				Not Measured								
PC-LN	2±0.01												

TABLE 3.3.1. RAW DATA PHASE II SPECIMENS (Continued)

Device Type	SCS-476	1	2	3	4	5	6	7	8	9	10	11	12
						MEASURED DATA							
						3.10.4 τ x β							
BP-Q	4.03	4.03	4.03	4.03	4.03	4.30	4.03	4.03	4.03	4.03	4.03		
BP-LN	60	60	60	60	60	60	60	60	60	60	60	60	
TDL-100	127	127	127	127	127	127	127	127	127	127	127		
TDL-200	127	127	127	127	127	127	127	127	127	127	127		
PC-Q						Not Measured							
PC-LN													
						3.10.5 L_{ins} (dB)							
BP-Q	20±2	–	22	–	21	21	–	22	21	21	21		
BP-LN	20±1.5	18	Detuned	19	19	19	19	19	19	19	19	19	
TDL-100	27±3	29	29	29	28	29	28	29	28	28	28		–
TDL-200	26±3	27	27	27	27	26	26	27	26	27	26	27	–
PC-Q	50±5	47	47	47	47	48	49	48	47	47	–		
PC-LN	30±3	29	29	28	33	Broken Bond Wire	29	28	28	29	29	29	28
						3.10.6 $S_{s.l.}$ (dB)							
BP-Q	≥35	–	39	–	35	39	–	36	36	35	–		
BP-LN	≥35	39	Detuned	40	40	37	38	38	40	40	–	–	
TDL-100	≥17	18	18	17	18	18	18	17	18	19	19	17	–
TDL-200	≥17	15	14	15	14	16	16	16	15	15	12	15	15
PC-Q	≥25	32	33	30	33	32	30	33	31	33	31		
PC-LN	≥20/25	25	27	24	25	Broken Bond Wire	25	25	24	23	25	25	25

*Measured values are worst case for the first leading and trailing sidelobes. All others were 5 dB greater than the measured values.

TABLE 3.3.1. RAW DATA PHASE II SPECIMENS (Continued)

Device Type	SCS-476	1	2	3	4	5	6	7	8	9	10	11	12
						MEASURED DATA							
						3.10.7 $S_{f.t.}$ (dB)							
BP-Q	≥50	–	55	>60	>60	–	>60	>60	>60	>60	–		
BP-LN	≥50	>60	Detuned	>60	>60	>60	>60	>60	>60	>60	>60	>60	>60
TDL-100	≥50	–	–			33	–	34	–	–	40		
TDL-200	≥50	48	38	50	45	37	44	–	–	36	46	39	50
PC-Q	≥50	51	53	50	53	51	51	53	50	50			
PC-LN*	≥50	60	>60	>60	>60	Broken Bond Wire	>60	58	>60	59	59	58	–
*Dynamic range of oscilloscope was 60 dB.													
						3.10.8 S_{spur} (dB)							
BP-Q	≥35	–	49	–	43	35	–	32	49	39	–		
BP-LN	≥35	36	37	38	–	–	40	38	–	–	–	–	
TDL-100	≥35	–	–	–	–	33	–	43	–	–	40	–	–
TDL-200	≥35	38	36	40	35	31	28	–	–	35	33	40	40
PC-Q	≥35	49	50	52	53	51	53	52	53	55	53		
PC-LN	≥35	31	34	25	31	Broken Bond Wire	25	29	26	29	30	29	25
						VSWR – Input Transducer							
						3.10.9 N:1							
BP-Q	≤2:1	1.1	1.1	Broken Bond	1.12	1.28	3.6	1.02	1.18	1.18	–		
BP-LN	≤3:1	1.93	2.1	1.79	1.79	1.79	1.79	1.93	1.93	1.93	1.79	1.95	
TDL-100	≤4:1	2.1	2.34	2.34	2.1	2.1	2.34	2.1	2.34	2.1	2.1	2.1	–
TDL-200	≤3:1	2.6	2.34	2.02	3.6	2.02	1.79	1.93	2.34	1.67	2.6	2.52	2.5
PC-Q	≤2.5:1	1.5	1.5	1.57	1.5	1.57	1.5	–	1.5	1.5	–		
PC-LN	≤3.5:1	4.1	4.1	4.1	4.0	4.0	4.2	4.0	4.0	4.0	4.2	–	3.8

TABLE 3.3.1. RAW DATA PHASE II SPECIMENS (Continued)

Device Type	SCS-476	MEASURED Data 1	2	3	4	5	6	7	8	9	10	11	12
		VSWR – Output Transducer 3.10.9 N:1											
BP-Q	≤2:1	1.18	1.28	Broken Bond	1.33	1.2	–	1.26	1.13	1.18	–		
BP-LN	≤3:1	1.93	1.93	1.93	1.93	1.93	1.93	1.93	1.93	1.93	1.93	1.93	1.93
TDL-100	≤4:1	2.6	2.02	1.93	1.67	2.02	1.72	2.02	1.67	1.72	1.67	1.79	1.93
TDL-200	≤3:1	2.1	2.6	2.5	1.93	2.5	2.5	2.5	1.85	2.34	1.93	1.85	2.1
PC-Q	≤2.5:1	2.0	1.93	2.1	1.93	2.1	1.93	2.1	–	2.1	2.1	–	
PC-LN	≤3.5:1	2.1	2.1	2.65	2.45	2.45	2.45	2.45	2.45	2.45	2.45	2.45	2.45

TABLE 3.3.2. PERCENTAGE PASSING PRECAP TEST

	BP-Q	BP-LN	TDL-100	TDL-200	PC-Q	PC-LN
f_o	100 (9)	100 (11)	100 (12)	100 (12)	100 (10)	100 (12)
β	100 (8)	100 (11)	–	–	–	–
τ	100 (8)	100 (11)	100 (12)	100 (12)	–	–
$\tau x \beta$	100 (10)	100 (11)	100 (10)	100 (10)	–	–
L_{INS}	100 (7)	90 (10)	100 (10)	100 (10)	100 (9)	100 (11)
S_{sl}	100 (6)	100 (8)	100 (10)	0 (10)	100 (10)	100 (11)
S_{ft}	100 (6)	100 (11)	33 (3)	20 (10)	100 (10)	100 (10)
S_{spur}	33 (6)	100 (9)	67 (6)	60 (10)	100 (10)	0 (11)
VSWR-Input	86 (7)	100 (11)	100 (11)	92 (12)	100 (8)	0 (12)
VSWR-Output	100 (7)	100 (11)	100 (12)	100 (12)	100 (8)	100 (12)

Notes:

1. Numbers in parenthesis indicate numbers of devices tested.
2. Shaded areas indicate less than 100% acceptable.
3. "Dashed" parts and parts with mechanical failures (open, broken bond wire, and detuned) were not included in this data.

TABLE 3.3.3. CORRECTIVE ACTION FAILURE ANALYSIS SUMMARY FOR PHASE II SPECIMENS

	BP-Q	BP-LN	TDL-100	TDL-200	PC-Q	PC-LN
f_o						
β						
τ						
$\tau x \beta$						
L_{ins}		Retuned – See Discussion				
S_{sl}				Reverse Code Line $f_o \neq 200$		
S_{ft}			Test Fixture, Ground Pad	Test Fixture Ground Pad		
S_{spur}	Insufficient RTV on XTAL ends		Same as S_{ft}	Same as S_{ft}		RTV on Shunt Resistor
VSWR-Input	Retuned – Excess RTV in Toroid			Toroid Substitution – See Discussion		Series R Omitted from Mask
VSWR-Output						

Lithium Niobate Linear Phase Bandpass Filter (BP-LN)

Serial Number 1 missed the insertion loss specification by 0.5 dB on the low loss side. All the BP-LN devices tended to have insertion loss at the low end of the newly specified range. This is a result of the fact that the series tuning inductor which was on the "hot" side of the output transducer during Phase I, was moved to the ground side in Phase II. This change produces a decrease in insertion loss of about 2 dB because ground side inductors, unlike hot side inductors, do not produce a reduction in the effective radiation resistance of the transducers. Note that it is not always desirable to use ground side inductors because they can be detrimental to the (spurious) electromagnetic feedthrough. In the case of the BP-LN, this was not a problem. The reason for moving the output inductor to the ground side was for ease in wiring the device, whose crystal layout was designed for input and output on opposite sides of the header, while the Tekform 20221 header requiring input and output on the same side was used for Phase II.

S/N 1 was brought into specification by adjusting the tuning toroids.

Quartz Biphase Coded Tapped Delay Line Filters (TDL-100 and TDL-200)

Both devices will be treated together, since corrective actions were the same for both devices:

1. All of the TDL-200 devices failed to meet S_{sl} by one to five dB. The center frequency of the reverse coded line was found to be incorrect, causing this sidelobe problem. During test demonstration, suitable sidelobe response was demonstrated by elevating the temperature of the reference line, thereby adjusting f_o. A reverse coded line of the proper frequency was fabricated for shipment to ERADCOM.

2. None of the TDL-100 or TDL-200 lines met the feedthrough (S_{ft}) or spurious (S_{spur}) specification. Failure to meet the feedthrough specification by up to 15 dB was attributed to unanticipated wear in the test fixture. It was found that various manual adjustments in pressure and position of the package in the fixture would momentarily bring the device into specification. The test fixture in Figure 3.2.9 was fabricated to resolve this problem. In addition, a ground pad was superimposed between input and output transducers at the photomask level in order to further enhance feedthrough suppression for Phase III.

3. One out of twelve devices failed the input VSWR specification. In addition, it was noted that the remainder of the devices were marginal, and the feedthrough VSWR tuning procedure was difficult. As a result, a plastic core (T16-10) toroid with lower permeability than the iron core (T16-0) used previously (but an increased number of turns to produce the same inductance) was substituted at the input transducer. The larger number of turns was more evenly distributed around the plastic core making the VSWR tuning procedures easier. It should be noted that cores with tightly clustered windings were noted to be more sensitive to coil orientation than evenly distributed turns with regard to feedthrough.

Substitution of the iron core with the plastic core undoubtedly aided the out of specification feedthrough on the TDL devices. A series of experiments were conducted to elucidate these relationships which are discussed at length in Appendix X.

Lithium Niobate Pulse Compression Filter (PC-LN)

1. All of the PC-LN devices failed the spurious specification by as much as 10 dB. Examination of the data indicated that the source of the spurious signal was not a result of triple transit phenomena. In addition, on the failed devices it was noted that a bead of RTV had been placed across the ends of the crystal on the top surface, which normally adequately supresses the spurious resulting from end reflections. However, it was noted that the PC-LN had an integral shunt resistor on each transducer which was not covered with RTV. See Figure 3.3.1. Upon reworking a number of these devices during test by coating the shunt resistor with RTV, the spurious suppression specification was met. There are two possible reasons for the improved spurious echo suppression with additional RTV placed over the thin film shunt resistor. The first is that the unacceptable spurious echo was reflected from the ends of the crystal and it had not been possible to suppress it adequately with RTV placed only near the crystal ends and outside the shunt resistor. The second is that the reflection arose from the shunt resistor itself as shown in Figure 3.3.1. It is fairly well established that a single stripe of aluminum on lithium niobate produces a reflection at the -44 dB level, which should not be large enough to violate the spurious echo suppression specification. However, it would be advisable in the future to design shunt resistor films so that the end segment, which reflects surface waves, is inclined at an angle of about ten degrees with respect to the transducer electrodes, so that the reflected wave will be diverted to the side.

2. All input transducers on the PC-LN's failed the 3.5:1 input VSWR specification by as much as 4.2:1. Excessive VSWR levels on the input transducer were traced to the use of a defective mask. In the generation of a modified mask for Phase III array size requirements, the series tuning resistors were inadvertently omitted. A new mask was fabricated in order to correct this deficiency.

3.4.0 MATERIALS AND PROCESSING CONSIDERATIONS FOR PHASE II DEVICE FABRICATION

This section will be divided into three segments approximating the process flow actually encountered in the fabrication of a device. The first will address the fabrication of new masks for Phase II and a summary of changes required. This will be followed by a section on wafer fabrication and related problem areas. Finally a section will be devoted to problems related to header assembly.

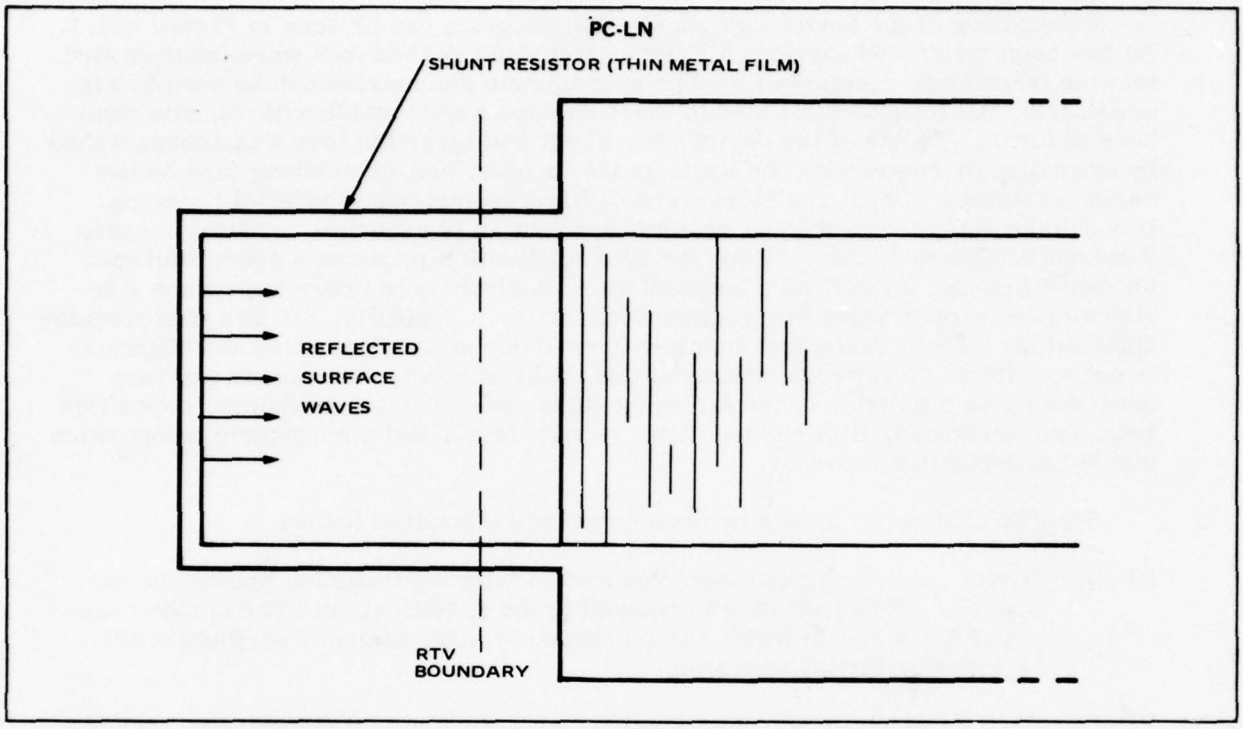


Figure 3.3.1. Schematic of PC-LN Transducer with Shunt Resistor

3.4.1 Mask Fabrication

Schematics of the device layouts for this program can be seen in Figure 3.4.1. As has been mentioned earlier, all series and shunt resistances were incorporated into the transducer design itself. The approximate geometries can be seen in Figure 3.4.2. All inductors utilized in these designs were toroids with various numbers of turns. Tuning of the devices for VSWR and insertion loss was accomplished by expanding or contracting the turns on the toroids, and/or scribing taps on the series resistors. Shunt resistors were of fixed geometry on the PC-LN device. It should be noted that the shunt resistor application is especially critical because it cannot be adjusted later. Also, the SAW application requires a given thickness for mass loading, as well as a constant sheet resistivity in order to produce a resistor of the proper value for a constant geometry. Typically, for thin film resistor applications a sheet resistance monitor is used during the deposition and thickness is not specified. Sheet resistivities of thin films of constant thickness can vary quite widely as a function of the following variables: surface roughness, deposition rate, film thickness, film composition, vacuum level, and atmospheric composition inside the deposition chamber.

Specific changes to masks by device type are discussed below:

BP-Q: Series resistor values were reduced to improve insertion loss at the expense of VSWR, which was relaxed in the specification. The scribe channel (Figure 3.4.2) width was increased to make diamond scribing of the taps easier for the operator.

BP-LN: Scribe channel width was increased with concomitant decrease in resistor line width to maintain the same resistance value per tap.

PC-Q: Series resistance values were doubled to optimize insertion loss, and scribe channel width was increased.

PC-LN: The shunt resistance value was doubled to increase the distance, D, in Figure 3.4.2. This was necessary to allow the assembler enough space to get a sufficient amount of RTV over the resistor to maximize spurious rejection without getting RTV on the fingers at the end of the transducer. A compatable increase in series resistance was also required, and the scribe width was also increased.

TDL 100 and 200: As discussed in Section 3.2.0, the metallization thickness of the TDL devices was reduced to improve spurious echo suppression and sidelobe suppression. As a result, the geometries of the series resistors had to be changed to effect the same resistance value. In addition, the scribe channel width was increased and a ground pad added between transducers to improve feedthrough. The latter required an increase in the transducer spacing of 100 mils. A reverse coded transducer was also added to the mask in order to be able to produce both device types with one mask.

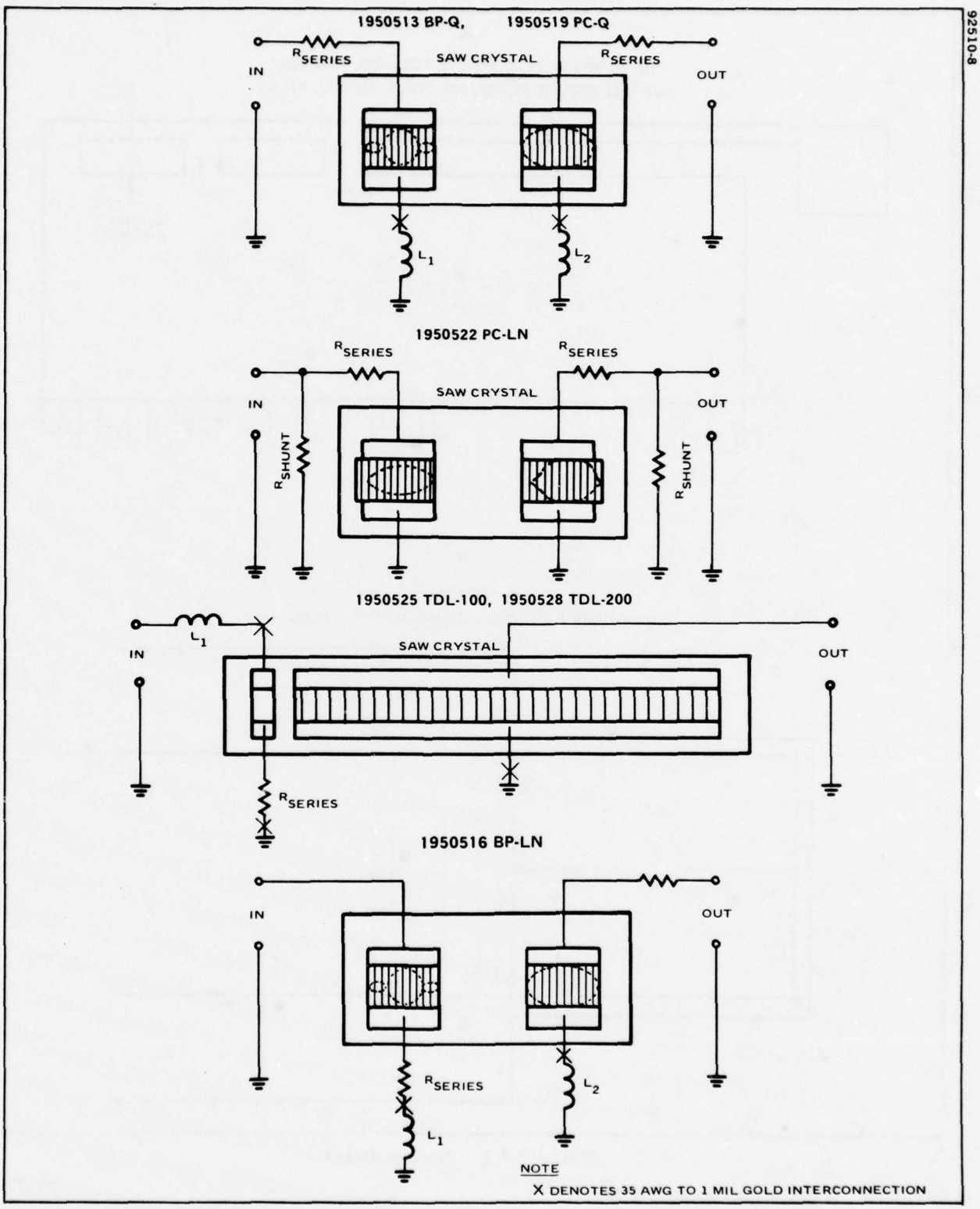


Figure 3.4.1. MMT SAW Device Schematic Representation of Device Layouts in Figure 3.2.9

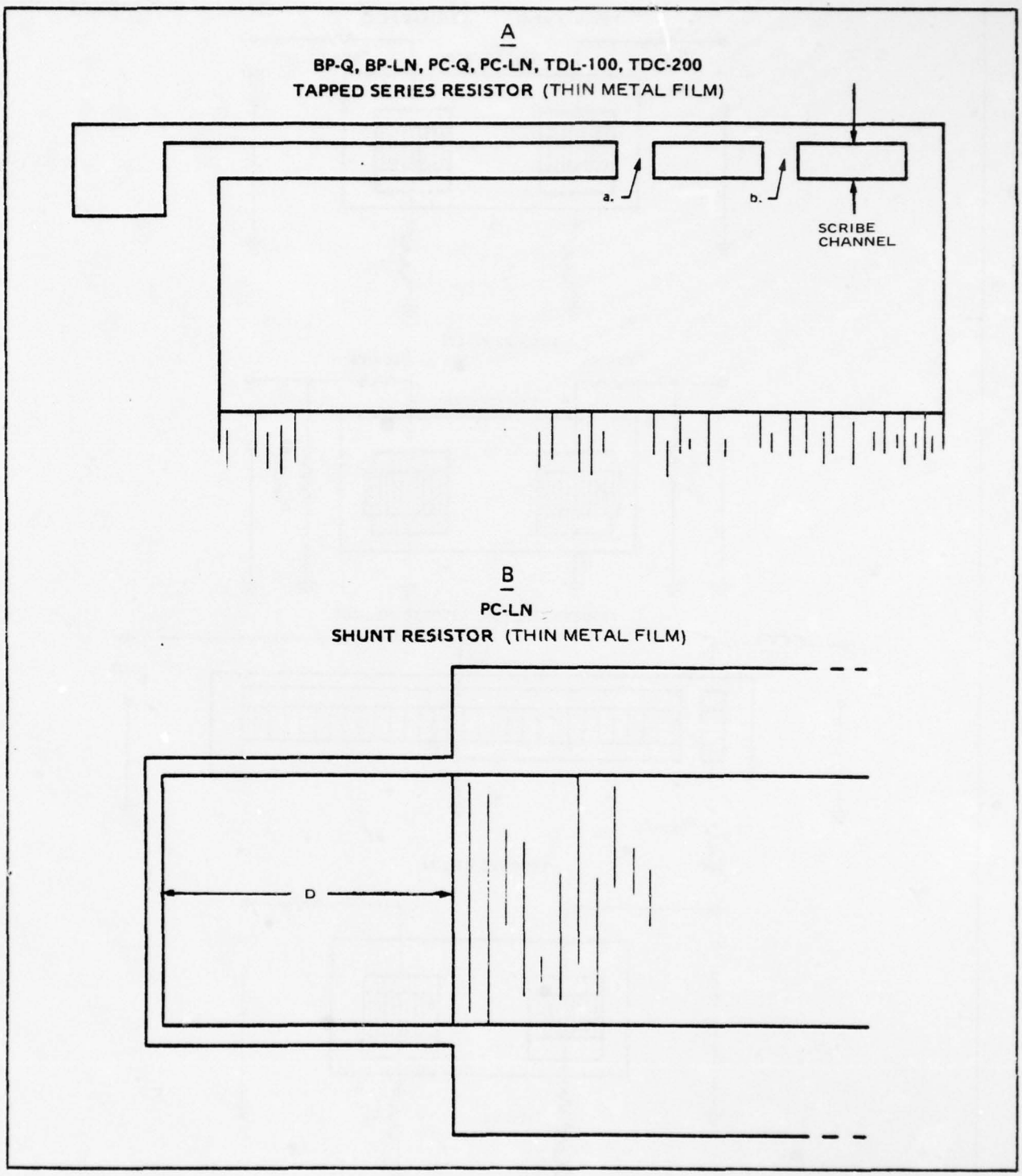


Figure 3.4-2. Resistor Detail

All devices were restepped in arrays which filled the wafer sizes chosen for this program (2"x2"x0.025" ST Quartz and 2.1"x1.75"x0.020" YZ $LiNbO_3$) utilizing a 0.006 in. channel to accommodate the anticipated kerf loss resulting from the diamond sawing operation, utilizing the new Electroglass dicing saw. A summary of individual die and array sizes can be seen in Table 3.4.1.

TABLE 3.4.1. INDIVIDUAL DIE TYPE, SUBSTRATE MATERIAL, SIZE, ARRAY SIZE, DIE/WAFER

Designation	Substrate	Individual Device Size	*Final Array Size	Die/Wafer	
				Phase III, IV	Required Per SCS 476
BP-Q	ST Qtz.	.586" x .172"	3 x 11	33	15
BP-LN	YZ $LiNbO_3$	.500" x .200"	4 x 8	32	15
PC-Q	ST Quartz	.800" x .200"	2 x 10	20	10
PC-LN	YZ $LiNbO_3$	.650" x .115"	3 x 15	45	10
TDL-100	ST Quartz	2.0" x .220"	1 x 9	9	7
TDL-200	ST Quartz	2.0" x .155"	1 x 12	12	7

*Size array which will fit on 2" x 2" ST Quartz or 2.1" x 1.75" YZ $LiNbO_3$.

Dicing guides were also changed from a continuous line to "cross hair" points at the corners of each die to eliminate the continuous metal stripe, which was felt to contribute to the degraded feedthrough of the Phase II devices.

All masks were made using an Electromask Image Repeater with a software package which allows it to be used as a fixed reticle pattern generator. Reduction steps were 10X, requiring a field of focus of 8 mm at 1X. Hard AR chrome, master grade blanks from Optifilm Inc., Gardena, Cal., were used for the 1X masters. It should be mentioned that the use of chrome (which allowed only one flash per second using the mercury source), and the large transducer size (>8 mm at 1X) on some of the devices required run times on the Electromask equipment as long as four hours. With the numerous design changes and reticles required to produce masks for this program, close cooperation between the designer and mask manufacture was mandatory to prevent repeated iterations of a given mask. Also, due to the excessive run times, a higher defect level for some designs was tolerated since repairs were not possible at the time of this program. Mask repair equipment is now available (Florod Corp., Hawthorne, Cal.) and is recommended for large production runs of devices as complex as those encountered in this program.

3.4.2 Wafer Fabrication

As was mentioned in Section 2.5.2, Volume 2 of this report, crystal orientation problems were encountered with the quartz vendor (Valpey-Fisher Corp.). Quality problems were again encountered with this vendor on a lot of plates used to fabricate TDL devices. A high density of polishing pits 5-10 micron in diameter was noted and the plates were returned to be repolished.

Dicing of wafers continued to be a problem during this phase of the program, with the new Electroglass dicing saw. While the equipment was quite adequate for the lithium niobate substrates, problems were encountered with 2 mil and 6 mil blade failure on the quartz material. The manufacturer recommended a modification of the saw to slow the blade from 30,000 to 20,000 RPM. This modification was implemented, but problems were still encountered with blade breakage. A thicker blade (12 mil) was used (Felker, Inc.) in conjunction with optical pitch as a mounting medium, and the problem diminished. However, the mask "streets" were once again too narrow for the kerf loss, and excess chipping was noted on some designs (PC-LN and BP-Q). Process development was also required for the lithium niobate dicing. Initially, double backed adhesive tape was used to mount the wafers to the glass mounting plate. The tape adhesive was found to form insoluble deposits on the top surface of the crystal upon removal and post-dice cleaning. This mounting medium was discarded and the same optical pitch (R. Howard Strausberg, Co.) utilized for dicing of quartz wafers substituted.

3.4.3 Header Assembly

The first step in assembly of the header was soldering of toroids to posts used to interconnect the series inductors and transducers. See Figure 3.2.8 and 3.4.1. This requires the soldering on all devices except the PC-LN of a #35 AWG wire to a post 30 mils in diameter and 40 mils high without shorting the pin to the case or allowing solder to wick over the top of the pin in order to allow wire bonding to the top of the post. See Figure 3.4.3. This operation is quite tedious and operator sensitive when it is necessary to make a 360^{o} wrap required to satisfy Mil-Std 883-B. However, with training this process was a cost effective approach. Another possibility would have been the use of substrate pads which were both solderable and wire bondable. This approach would have had an undesirable cost impact, and the affect of the increased shunt capacitance was felt to be detrimental for some devices (post capacitance has been calculated to be on the order of 5 pf).

After the series inductor interconnect, ground interconnects are made by soldering on all devices. The PC-LN transducer ground is effected using moly tabs and gold wire bonding. All of these interconnects could have been made with the wire bonder if the header had been gold plated. Originally, a cost savings was thought to be attainable through the elimination of the extra gold plating. However, for small header orders the dual plating approach is not cost effective due to set up costs and use of non-standard processes by the vendor. Indeed, during Phase IV gold plated headers were mandated due to the use of projection welding for package closure.

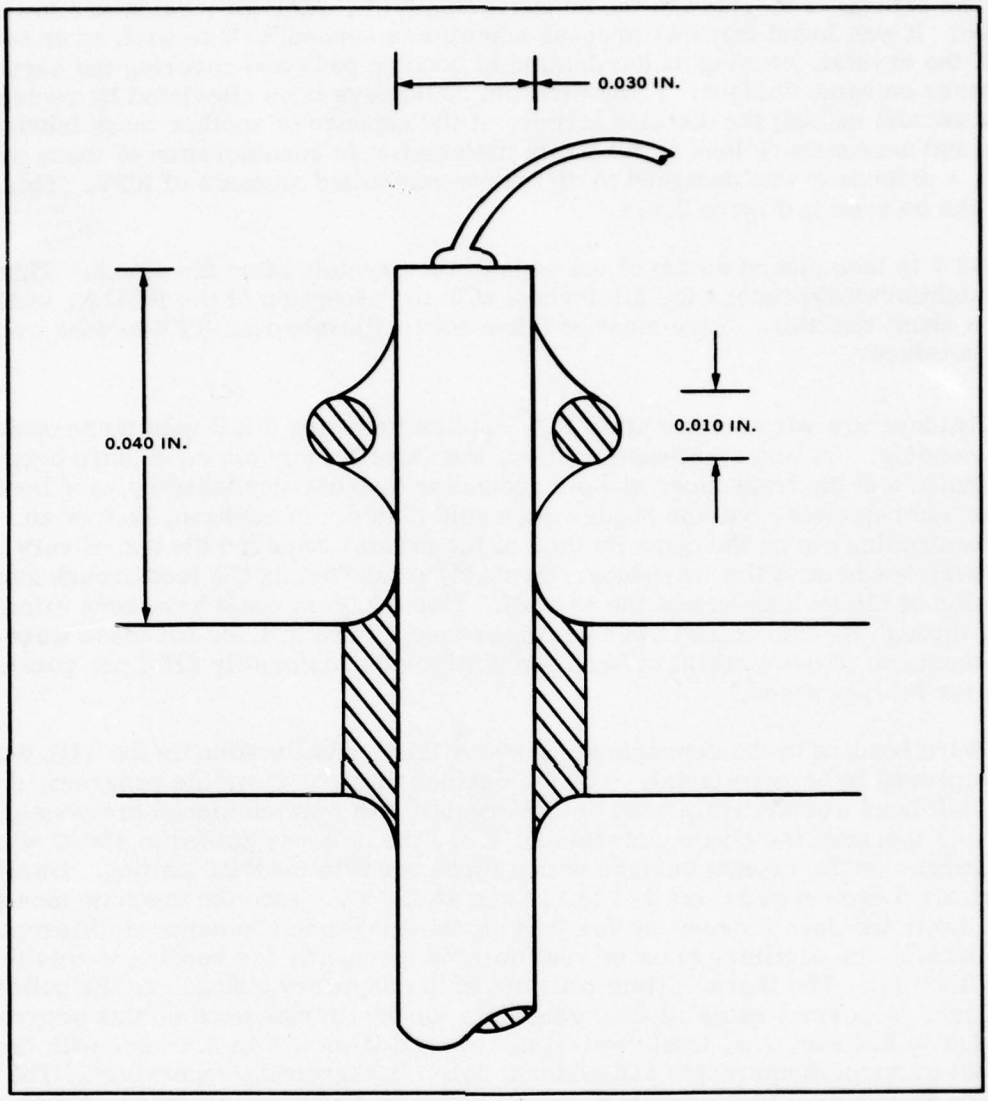


Figure 3.4.3. Schematic of Interconnect Post Utilized on BP-Q, BP-LN, PC-Q and TDL Devices (TDL Pin Diameter is 50 Mils)

The crystal is mounted to the header using RTV, after all toroids are installed. It was found that this process sometimes caused RTV to wick up on to the top of the crystal, causing contamination of bonding pads and covering the series resistors on some designs. (This problem could have been alleviated by restepping the mask and making the die size larger, at the expense of another mask fabrication cycle and unnecessary loss of substrate material.) In consideration of these problems, a dispenser was designed to distribute controlled amounts of RTV. This design can be seen in Figure 3.4.4.

RTV is then placed on top of the ends of the crystals after die attach. This is a straightforward process for all devices with the exception of the PC-LN, which uses a shunt resistor. Care must be taken not to allow excess RTV to wick over the transducer.

Headers are wire bonded after RTV application using 1 mil gold thermopulse wire bonding. As was mentioned earlier, the PC-LN moly tab could have been eliminated and the transducer and pin grounding step accomplished by wire bonding on the other devices, had the header been gold plated. In addition, lack of an interconnecting pin on the opposite side of the crystal required the use of very long wire bonds over the transducer, probably exacerbating the feedthrough suppression of all devices except the PC-LN. This problem could have been eliminated through the use of narrower packages (see Figure 3.4.5), but these were non-standard. Cost would have been prohibitive (approximately $15K per package type) for this approach.

Wire bonding to the approximately 500 $\mathring{A}$ thick metallization on the TDL devices proved to be non-trivial. For the devices fabricated on this program, the gold ball bond was always placed on the crystal. As was mentioned previously, this is a thermopulse bonding technique, i.e., the collet is pulsed to 450°C when it impinges on the crystal surface with a force equal to machine setting. Dwell times for these crystals was 1.4 to 1.6 sec at 450°C. Since the machine measures total dwell and does not account for varying thermal time constants of different capillaries, the capillary must be recalibrated frequently for bonding to this thin metallization. The thermal time constant of the capillary changes as the collet oxidizes. A normal range of time constants for capillaries used on this program was 1.1 to 2.1 sec, i.e. total dwell times ranged from 2.5 to 3.5 sec. with the crystal at room temperature and ambient collet background temperature. The optimized wire bonding schedule developed to pass requirements in paragraph 4.6.4.1 of Appendix IX utilized a reduced force from that normally used on the thicker metallization (a setting of 175 vs. 277 on the Hughes Thermopulse wire bonder). Unfortunately, this setting cannot be related to the number of grams force on this machine.

3.5.0 CONCLUSIONS FROM PHASE II

Engineering analysis was performed and/or device designs were modified on all six part types to reconcile performance with the modified specification. A packaging approach was developed which, although not optimized, met the requirements of the program as outlined in Appendix IX. These requirements were: hermeticity, low cost, ability to withstand thermal shock, pyrotechnic shock,

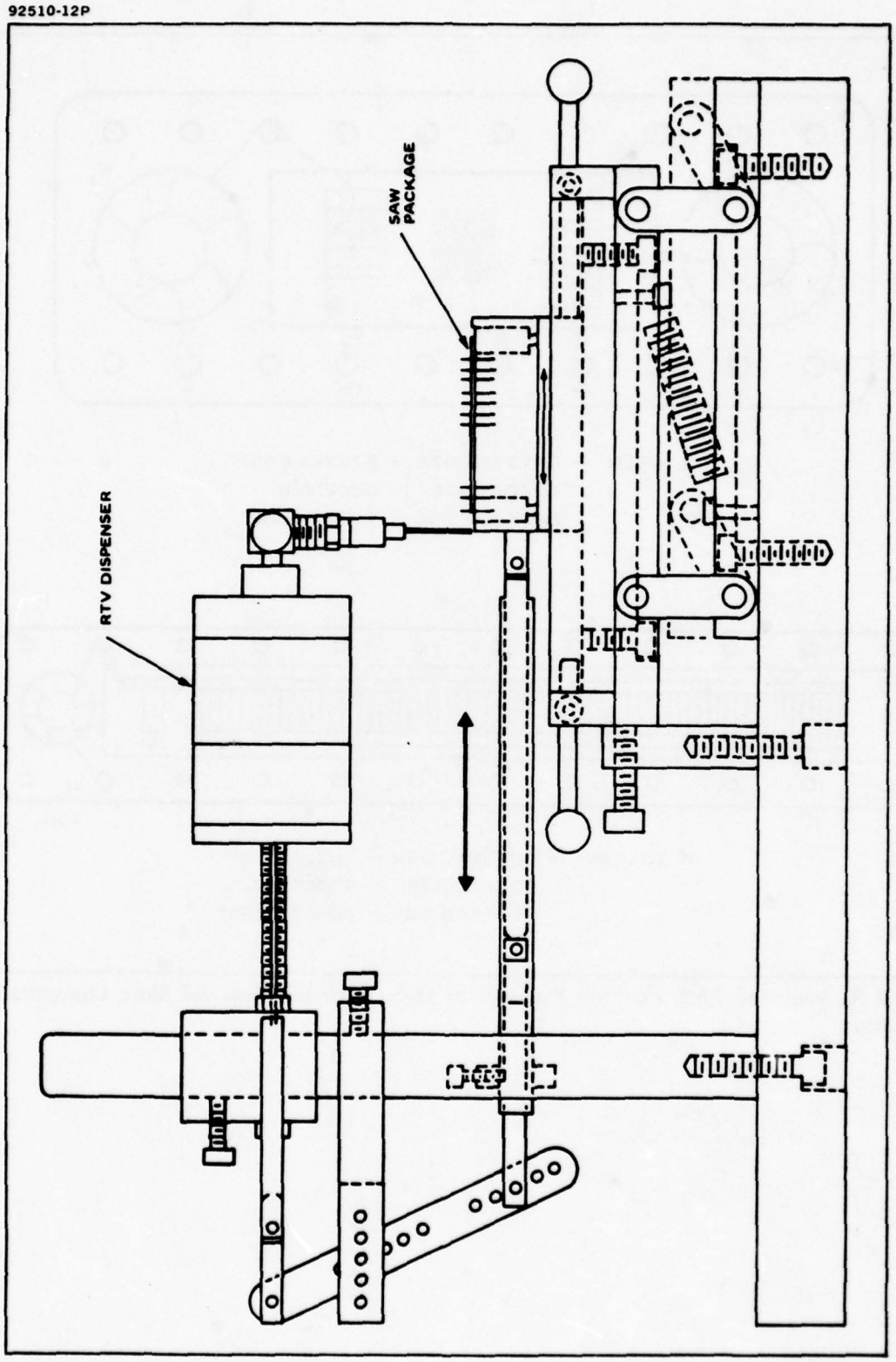


Figure 3.4-4. Dispenser for Application of Dow Corning 3140 RTV to Package Base

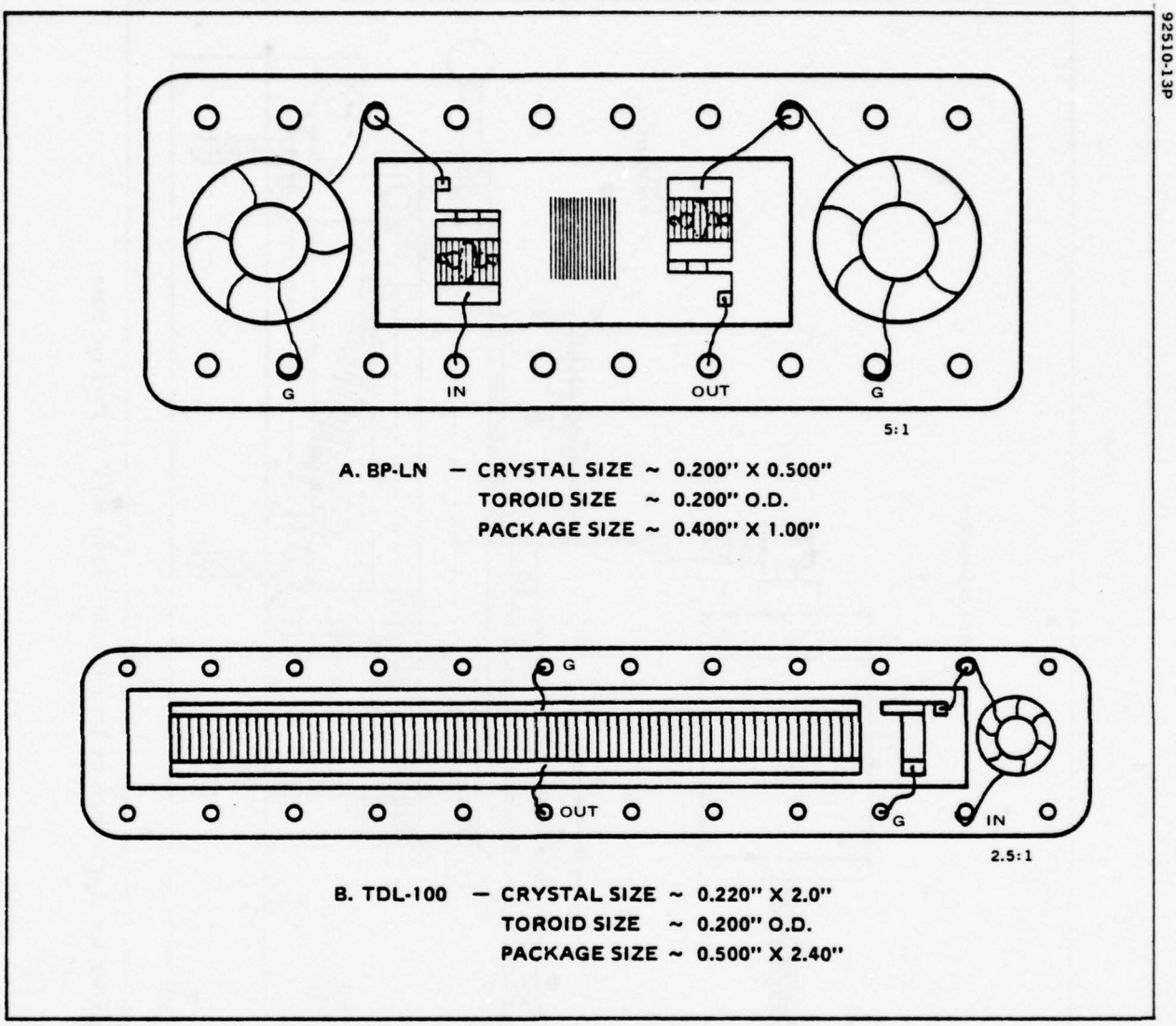


Figure 3.4-5. Proposed SAW Platform Packages of More Optimum Size and More Convenient Pin Configuration

vibration, moisture resistance, and the maximum outline dimensions of Table I, Appendix IX. Masks were restepped in arrays meeting the minimum requirements of Appendix IX, and batch photolithographic processing demonstrated.

Design and engineering data from the first two phases of this program demonstrated that a tight tradeoff exists between insertion loss and VSWR on these and similar designs. The specification was renegotiated for Phase II at the expense of VSWR, which was felt to be a reasonable tradeoff in view of the rationale developed in Appendix IV, Volume 2. Problems were encountered with devices in standard hybrid packaging vs. machined aluminum slotted assemblies in the form of difficulty in controlling and reproducing feedthrough suppression. Some of the variables noted in the feedthrough suppression problem were: toroid core composition, toroid winding size and orientation, a ground pad between transducers, and undoubtedly package design. Excess RTV in the center of the toroid core was noted to have a marked effect on insertion loss and VSWR. The shunt resistor design on the PC-LN was noted to act as a source of spurious rejection problems, and was cured only with a difficult RTV masking procedure. Lack of adjustability of the shunt resistor caused tighter control to be necessary on metallization sheet resistivity than on the other designs. Continuing problems were also encountered with ST quartz substrate quality and dicing of quartz using a high speed saw designed for silicon. Wire bonding schedule development for the 500 Å metallization on the TDL devices was tedious, but produced uniform acceptable quality once developed.

APPENDIX VII
ELECTRICAL TEST PROCEDURES AND EQUIPMENT UTILIZED IN PHASES I AND II

Center Frequency -f_o (SCS 476 para. 3.10.1)

While this is a frequency domain parameter, it is measured for TDLs and PC devices in the time domain because of greater accuracy, less operator dependence, and relative ease. The time domain measurement is accomplished by summing the output response from the device under test (DUT) with the output of the generator which supplies the original signal using a differential preamplifier in the oscilloscope. When the two signal input amplitudes are exactly the same, but 180^o out of phase, cancellation takes place and the precise frequency can be read from the signal generator or synthesizer. Figure 1 illustrates how this is accomplished for PC and TDL devices. When both signals are inserted into the scope preamplifier simultaneously and the center frequency of the signal source and the line stretcher are alternately adjusted for optimum null in the center of the presentation the exact center frequency can be read from the center frequency readout of the HP8660 Synthesizer.

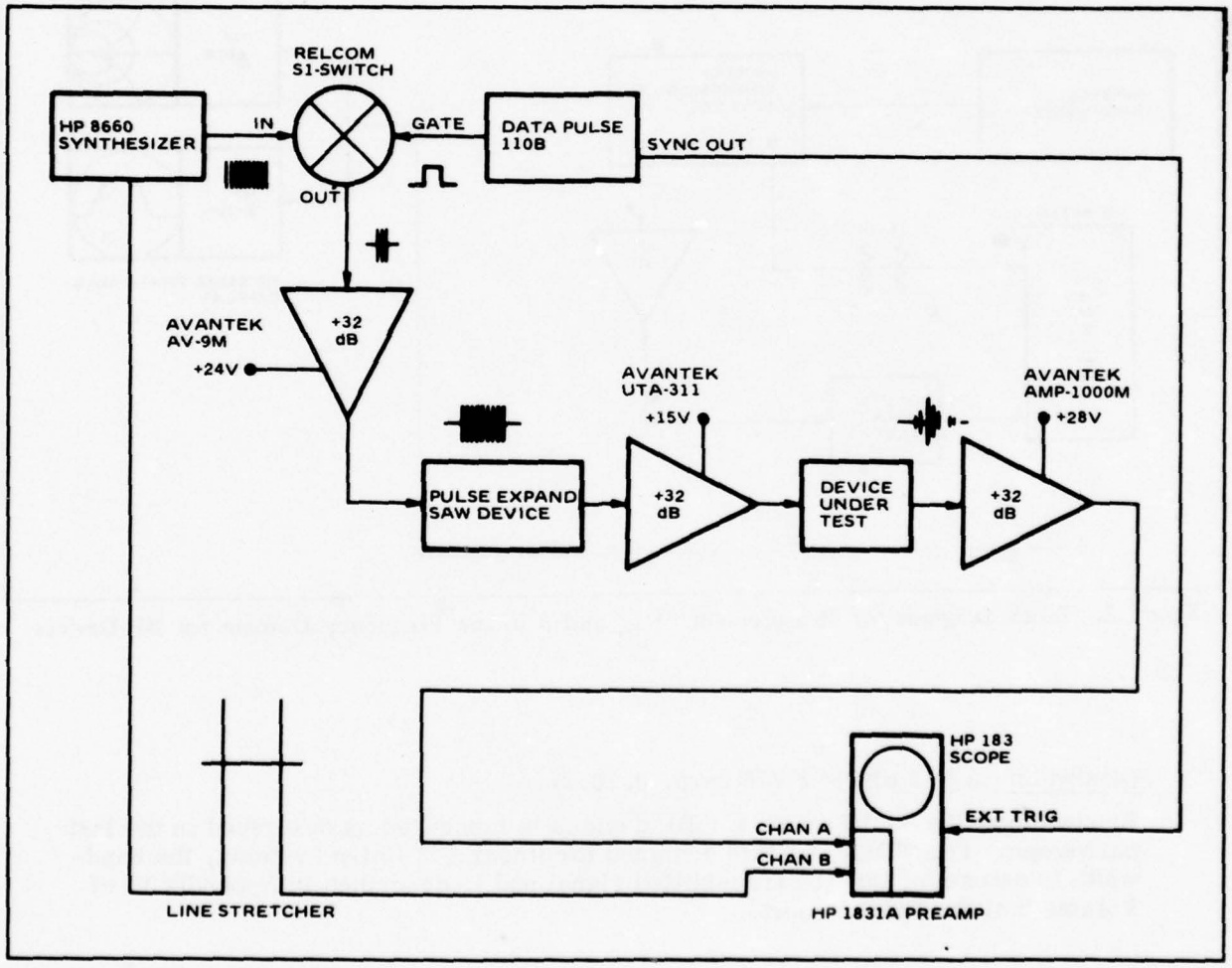


Figure 1. Block Diagram Measurement of Center Frequency (f_o) in the Time Domain for PC and TDL Devices

Center Frequency of bandpass filters (BP-Q and BP-LN) is measured in the frequency domain. Using the HP8410 Network Analyser in the transmission mode (Figure 2) with 1 dB/division amplitude sensitivity, the -3 dB points are measured on the high and low ends of the bandpass. The center frequency is then calculated as:

$$F_c = \frac{f_{HI} - f_{LO}}{2} + f_{LO}$$

This measurement simultaneously measures the 3 dB bandwidth (B) of the filter.

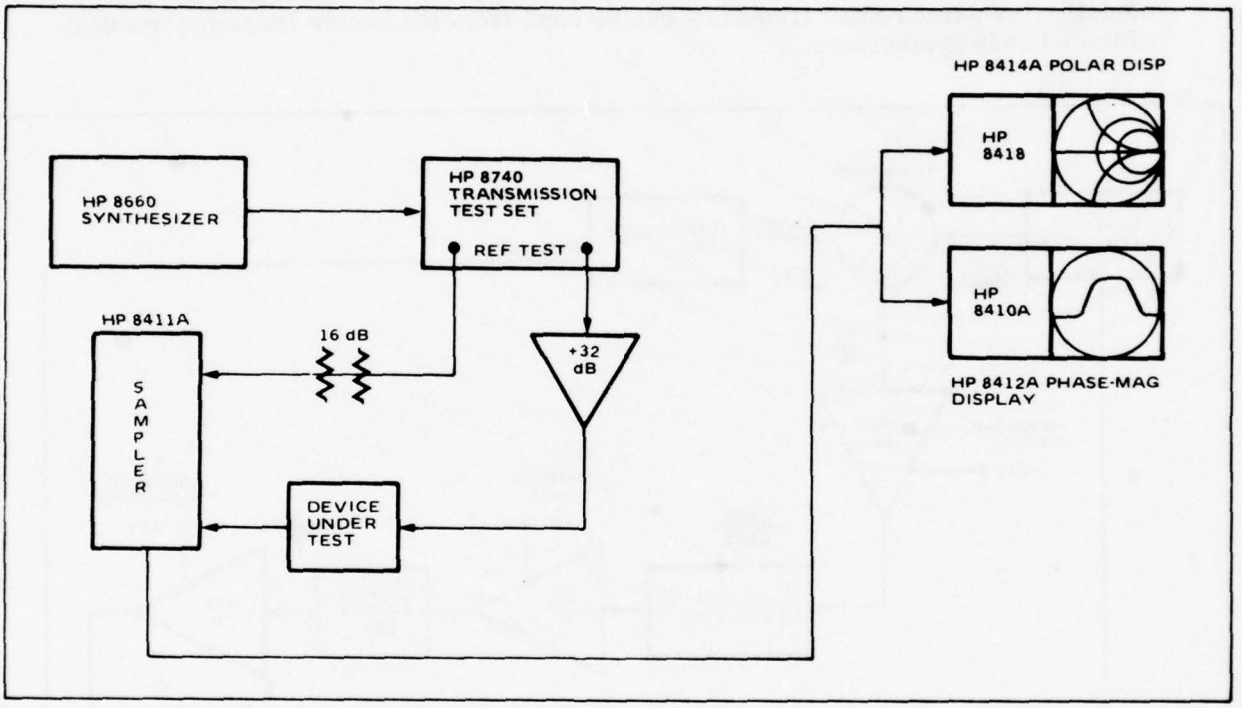


Figure 2. Block Diagram for Measurement of f_o and β in the Frequency Domain for BP Devices

Bandwidth – β @ -3 dB (SCS 476 para. 3.10.2)

Bandwidth at the -3 dB points for BP devices is measured as described in the last paragraph. For TDLs and PCs designed for linear FM Chirp Systems, the bandwidth is determined by the transmitted signal and is described in Appendix VI of Volume 2 of the Final Report.

Group Delay – τ (SCS 476 para. 3.10.3)

The group delay for BP devices is defined, and the Pi-Point Delay Measurement method is described in Appendix II of Volume 2 of the Final Report. In making this measurement, it is necessary to estimate τ and Δf in the equation below:

$$\tau = \frac{\Delta\phi}{360} \times \frac{1}{\Delta f}$$

$\Delta\phi$ is chosen in increments of N times 1, 2-1/2 or 10 degrees per division as dictated by the phase sensitivity adjustment on the Network analyzer. As τ is a design parameter of the device under test and is fixed by the photomask, Δf can be determined approximately by calculation in the formula above, e.g.:

$$\Delta f = \frac{\Delta\phi}{360 \times \tau} \quad \text{(chosen)}$$

The estimated Δf divided by 1000 is set as sweep width on the HP8660 synthesizer with the center frequency set to that of the filter and the results are observed on the horizontal display of the network analyzer. Both amplitude and phase are simultaneously displayed. Assuming $\Delta\phi$ is chosen to be 30^{o} and the analyzer is set for 10^{o} per division, the estimated Δf is varied until a series of intensified dots appear 3 divisions apart, lying parallel to the reticle in the flat phase response portion of the passband. (See Figure 3a) Δf is then determined by:

$$\Delta f = \frac{F}{1000}$$

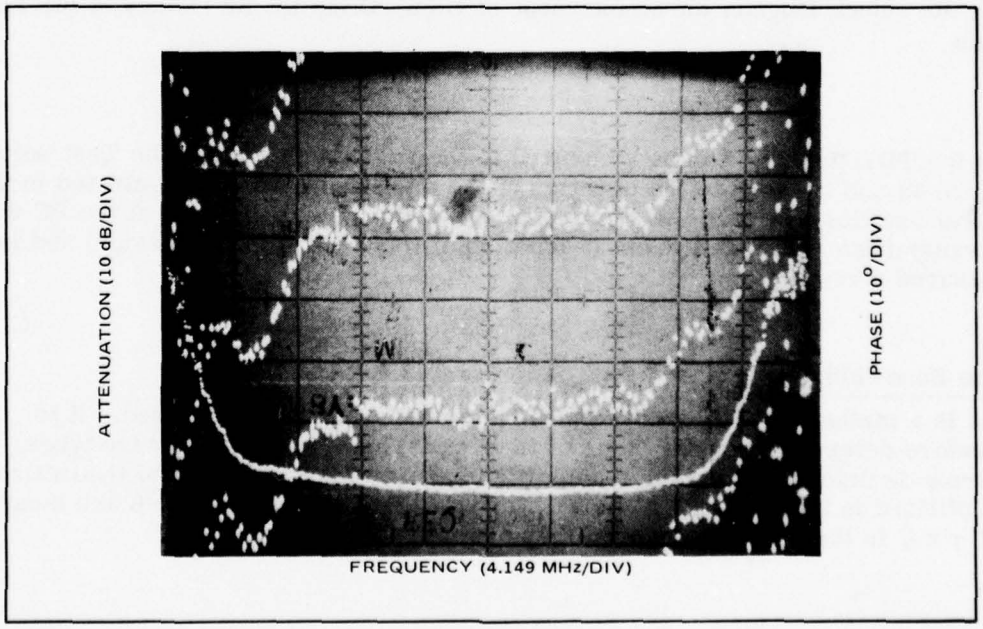


Figure 3a. Time Delay Measurement for BP-LN

where F is the sweep width (to the nearest KHz) read from the synthesizer. Substituting the values of ϕ and Δf determined above, τ can be calculated in microseconds. This test setup for BP devices can be seen in Figure 3b.

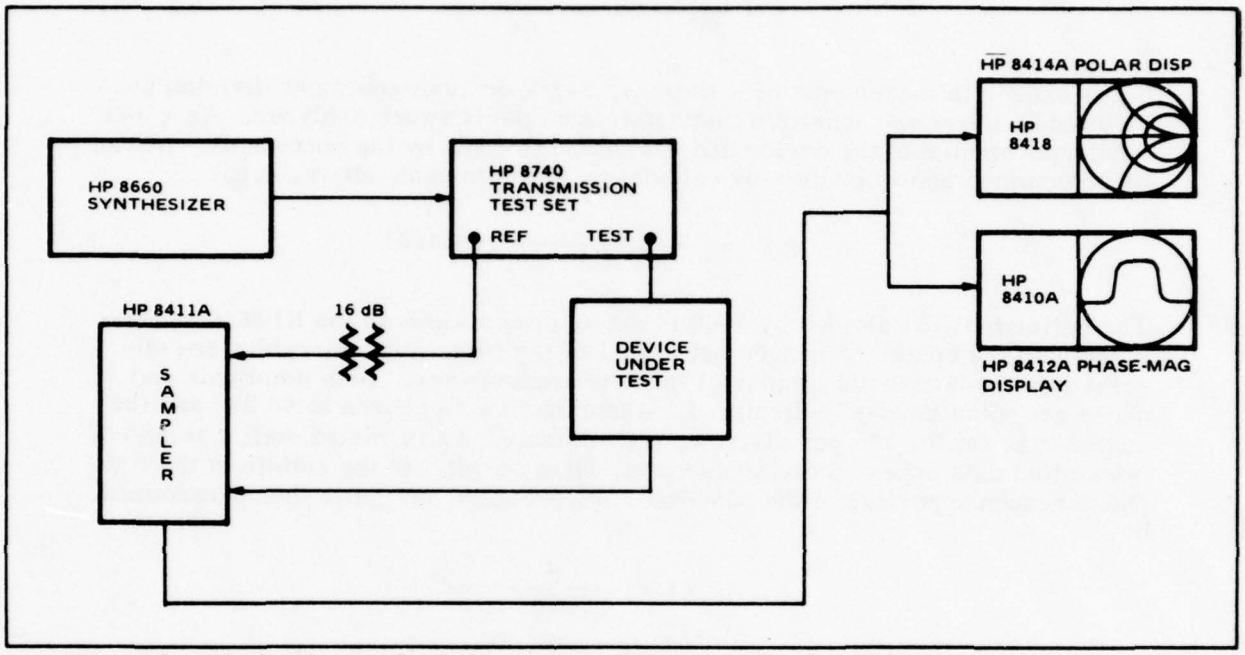


Figure 3b. Block Diagram for Measurement of Group Delay for BP Devices in the Frequency Domain

For the TDL lines, τ can be measured in the time domain using the Test setup in Figure 4a and is equal to the duration of the expanded pulse as illustrated in the typical oscilloscope trace in Figure 4b. As with the bandwidth, τ of the PC devices is transmitted signal dependent (a function of the expansion line design) and is not measured directly.

Time Bandwidth Product $-\tau \chi \beta$ (SCS476 para. 3.10.4)

This is a mathematically derived parameter and cannot be measured. It is therefore determined on the basis of theoretical τ and B for PC device types, where τ is determined by the transmitted signal. Measured τ and theoretical B are utilized in the TDL calculation . For BP devices, both τ and β are measured and $\tau \times \beta$ is the direct product of these two numbers.

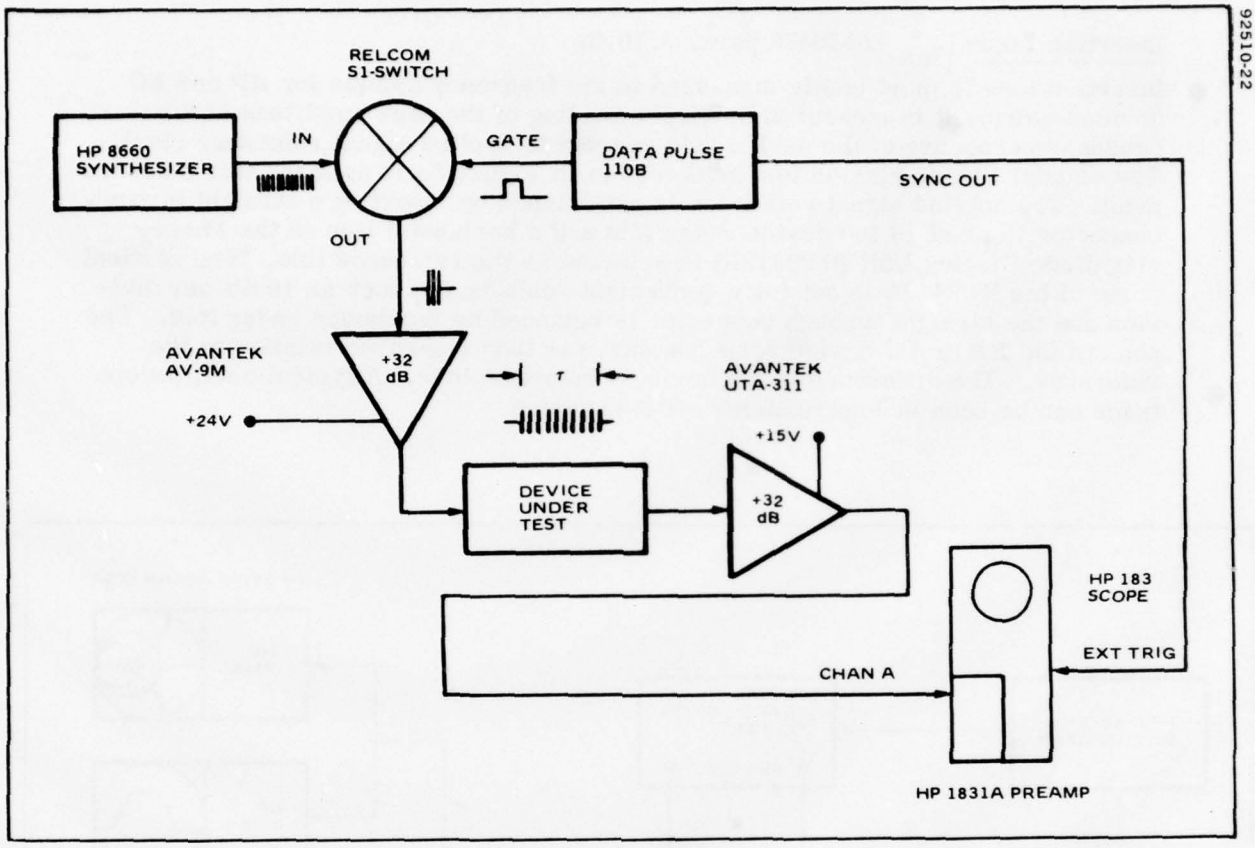


Figure 4a. Block Diagram for Measurement of TDL Group Delay in the Time Domain

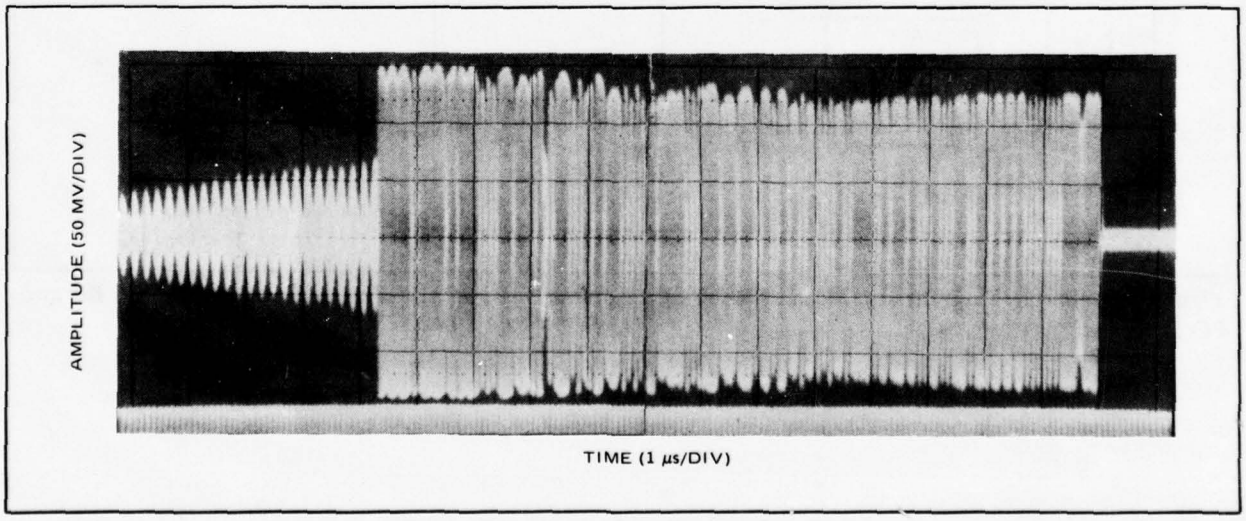


Figure 4b. Typical τ Display for TDL

Insertion Loss-L_{ins} (SCS476 para. 3.10.5)

Insertion loss is most easily measured in the frequency domain for BP and PC devices types. It is measured by direct reading of the peak amplitude of the bandpass respoonse of the device with respect to applied signal reference level. The standard transmission test setup shown in Figure 5a is used for this measurement. The applied signal reference is established by inserting a straight through connector in place of the device under test and a horizontal line on the Phase-Magnitude Display Unit (HP8412A) is selected as the reference line. The vertical scale of the HP8412A is set for a convenient scale factor such as 10 dB per division and the straight through connector is replaced by the device under test. The peak of the BP or PC device response curve is then measured relative to the reference. The difference is the device's insertion loss. A typical oscilloscope trace can be seen in Figure 5b for a BP-Q device.

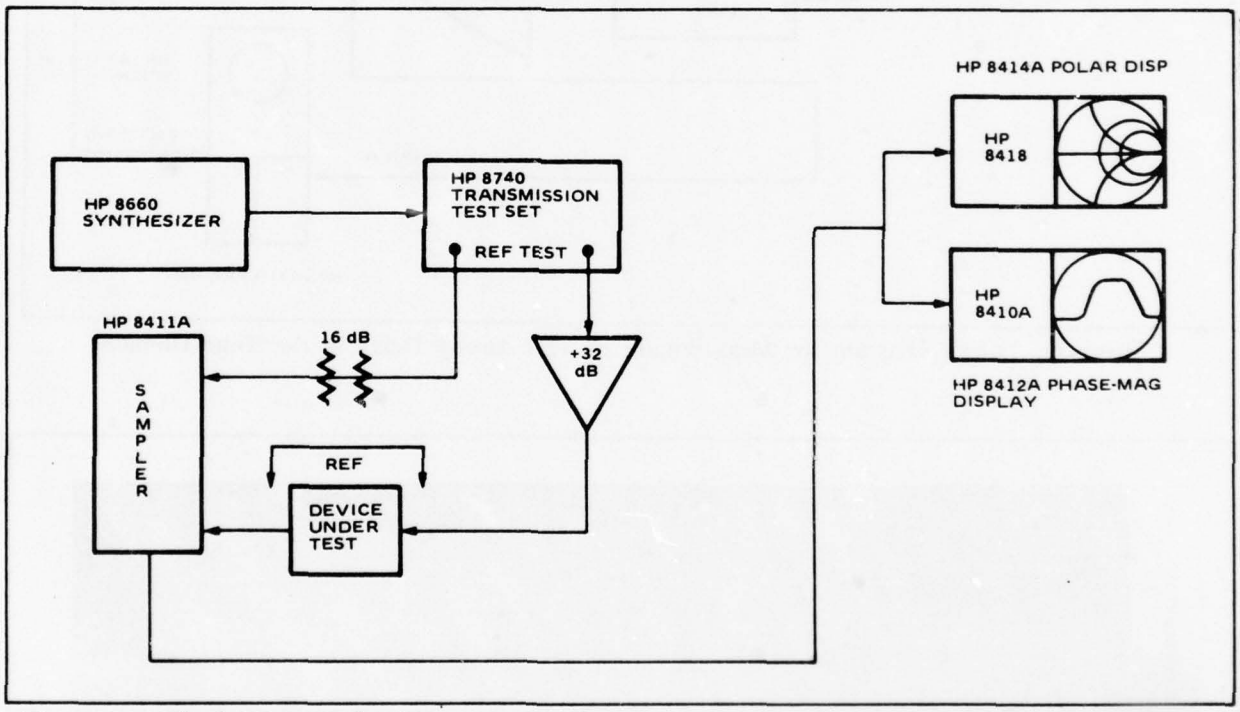


Figure 5a. Block Diagram for Measurement of Insertion Loss in the Frequency Domain for BP and PC Devices

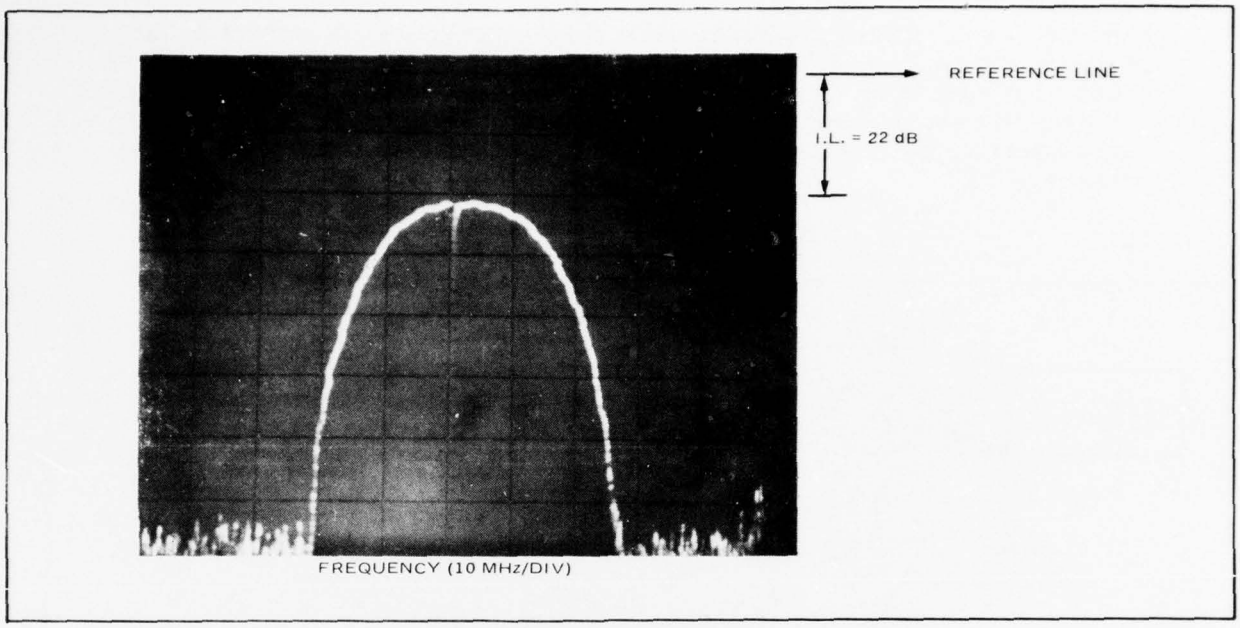


Figure 5b. Typical Insertion Loss Spectrum of BP-Q

In the case of the TDLs, the insertion loss is measured as follows: The matched biphase coded waveform is generated using a similar tapped delay line with the time reversed code polarity sequence. The waveform amplitude is limited using saturated amplifiers and then compressed in the tapped delay line filter under test. The insertion loss is the ratio of the input waveform amplitude to the amplitude of the correlation peak of the compressed pulse, expressed in decibels. See Figure 6.

Sidelobe Suppression-$S_{s\ell}$(SCS476 para. 3.10.6)

Sidelobe generation is a natural consequence of the type of process performed (device transfer function) on an incoming signal by a surface acoustic wave device.

For the TDL and PC filters, this parameter is measured in the time domain. A signal of the proper frequency, and pulse width is applied to the device under test to produce a full scale deflection of the desired signal on the oscilloscope presentation. The amplitude of the sidelobes is noted and the desired signal is attenuated using the Step Attenuators (HP355C and D) until its amplitude is precisely the same as the largest sidelobe. The change in the attenuator setting, or the amount of attenuation inserted, is the suppression in dB. The test setup to measure sidelobes for TDL and PC devices can be seen in Figure 6.

Sidelobes for BP filters are measured in the frequency domain and are defined to be any discontinuities, or irregularities, on the skirts of the filter bandpass response extending in either direction. The magnitude of the sidelobes is measured using the test setup of Figure 5a, and is the amplitude of the largest sidelobe with respect to the amplitude of the center frequency of the filter response expressed in dB.

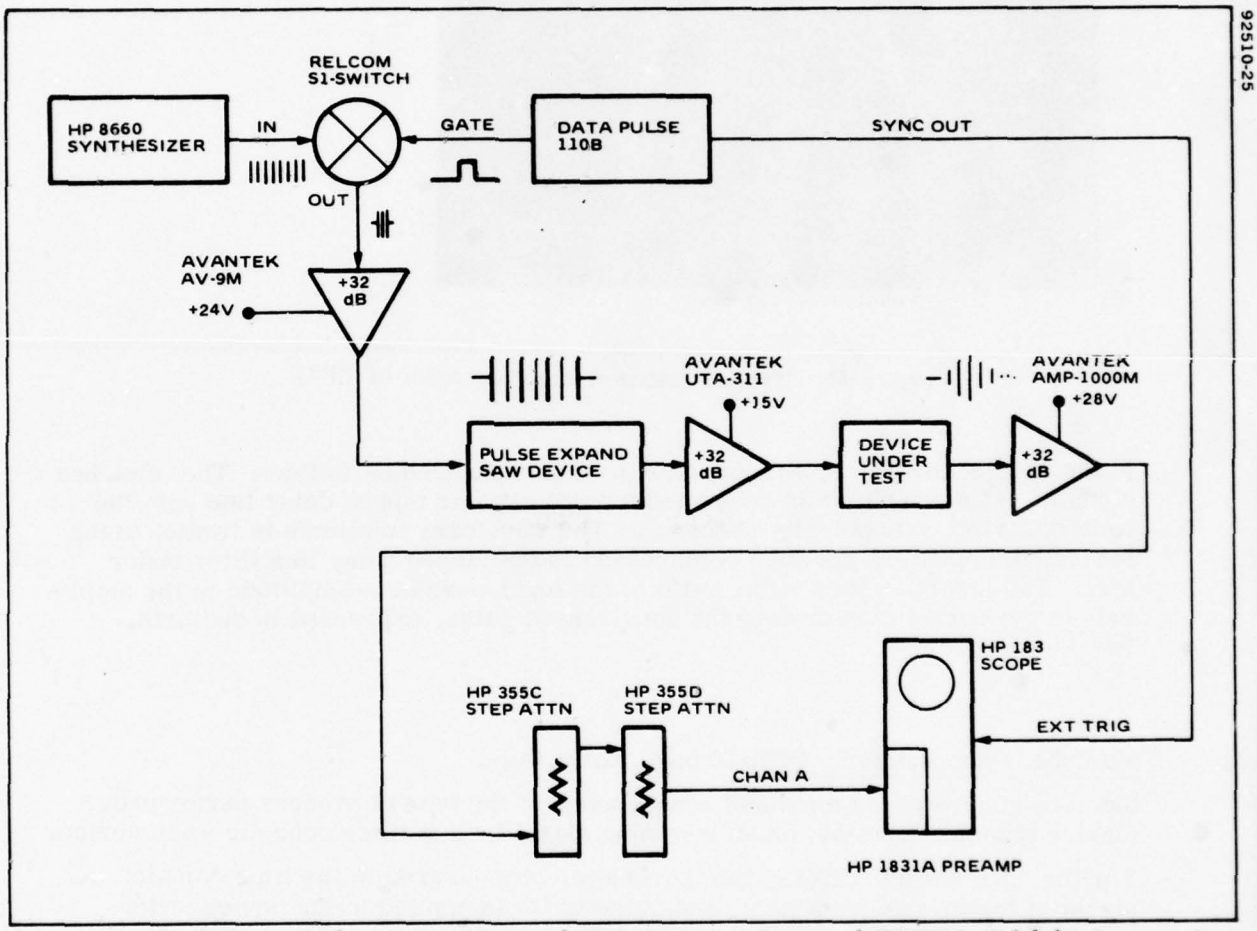


Figure 6. Block Diagram for Measurement of TDL Insertion Loss and PC/TDL Sidelobe Suppression in the Time Domain

Feedthrough Suppression – $S_{f.t}$ (SCS476, para. 3.10.7)

Feedthrough is a term used to express the amount of the original signal impressed upon the device under test which passes through the device without being altered by its transfer function. Since all signals processed by the device experience a time delay, the unprocessed feedthrough occurs earlier in time than the output response. An example can be seen in Figure 7 for a PC-Q device. Feedthrough suppression is then the difference in amplitude between the desired output (the processed or delayed pulse) and the original unprocessed signal, expressed in dB. A typical value for feedthrough suppression is 50 dB. As feedthrough results from the input signal bypassing the device, it is associated with device packaging and time delay (transducer proximity).

The measurement is made for PC, TDL and BP devices by adjusting the attenuators to set the feedthrough response to a convenient amplitude on the oscilloscope presentation and noting the magnitude of the feedthrough pulse. Adjust the HP355C and D attenuators in Figure 6 until the compressed pulse amplitude decreases exactly to the reference amplitude of the feedthrough pulse. The change in attenuator setting is the amount of feedthrough suppression.

Spurious Suppression – S_{spur} (SCS 476 para. 3.10.8)

Like sidelobe and feedthrough suppression, spurious suppression is most easily measured for all devices in the time domain. Spurious suppression is defined as the difference in amplitude between the desired signal and any undesired signal excluding feedthrough and sidelobes. In SAW devices, one major source of spurious signal is a result of reflections of the transmitted surface wave from the discontinuity represented by the transducer metalization. This type of spurious response has a precise relationship to the input, is equal to 3τ, and is called triple transit spurious (TTS). Other spurious signals result from reflections occurring at the ends of the crystal, or other discontinuities such as the shunt resistors on the PC-LN. These sources of spurious response are generally minimized by placement of an absorbing material such as RTV on the top surfaces of the crystal, and/or angling the crystal ends. While these sources have a relationship to the desired signal, it varies with device design and crystal size and type. An example of TTS in the time domain can be seen in the oscilloscope trace in Figure 7. Since sidelobes have a specific time relationship or duration with respect to the desired signal, spurious signals may be specified as undesirable signals so many microseconds beyond the carrier on either side. Sidelobes will be contained within the excluded time envelope. As an example, for a specific pulse compression filter those responses two microseconds and beyond on either side of the desired response are considered to be spurious. This is schematically depicted in Figure 7.

Spurious Suppression (or rejection) is measured by noting the difference between the largest spurious response and that of the desired signal. This is once again the change in step attenuator (HP355C&D) setting in Figure 6 required to reduce the amplitude of the desired response to that of the largest spur. Refer to the paragraph on feedthrough suppression for detailed description of this measurement.

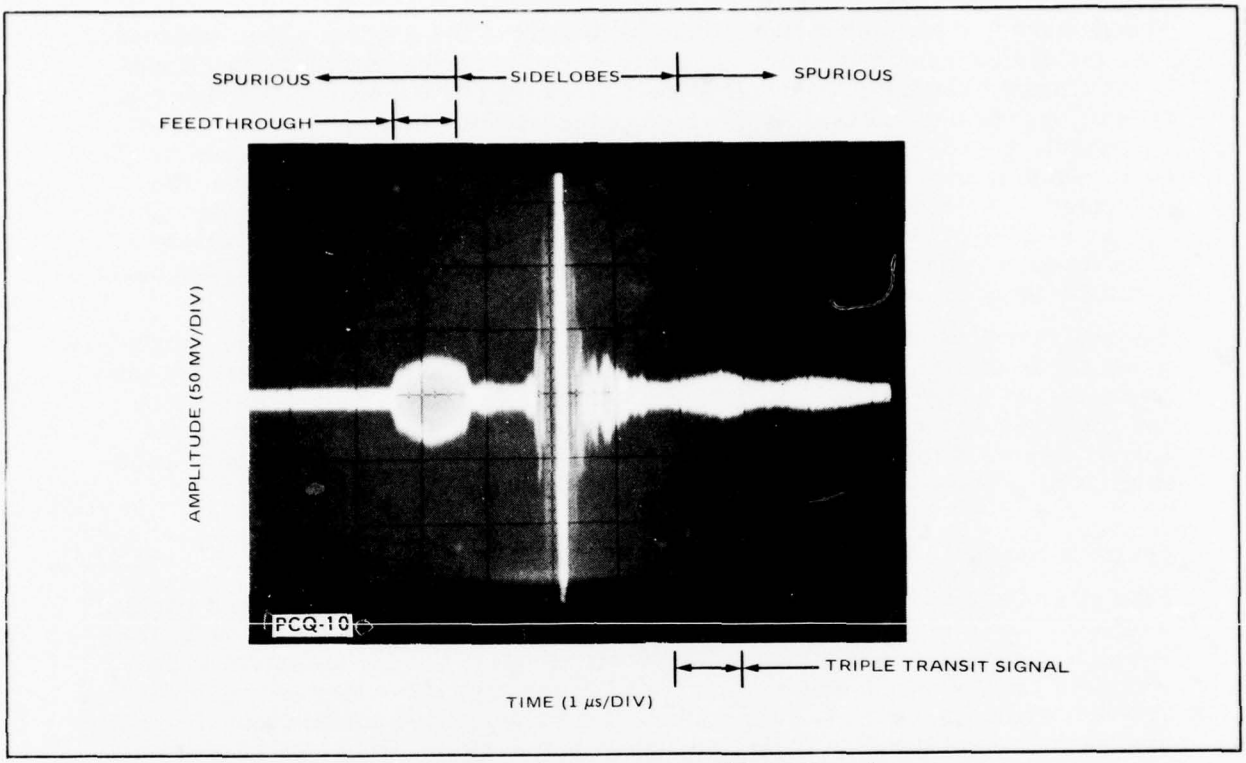


Figure 7. Typical Spurious, Feedthrough and Sidelobe Response for PC-Q in the Time Domain

Voltage Standing Wave Ratio – VSWR (SCS 476 para 3.10.9)

This parameter is measured for all devices in the frequency domain. Two types of display are possible. The first of these is the Smith Chart Plot which depicts the real and imaginary impedance and the magnitude of the mismatch. The second display is the magnitude of the reflected energy (return loss) as a function of frequency. This magnitude of the return loss is readily converted into VSWR by use of standard charts and nomographs, and requires only a standard oscilloscope, directional coupler and a sweep generator. An example of the test setup is shown in Figure 8, with a table of return loss versus VSWR. Typical data using both displays can be seen in Figure 9 for a BPQ device.

RTN LOSS dB	VSWR
1	18:1
2	8.8:1
3	5.9:1
4	4.4:1
5	3.6:1
6	3.0:1
7	2.6:1
8	2.34:1
9	2.1:1
10	1.93:1
12	1.67:1
20	1.25

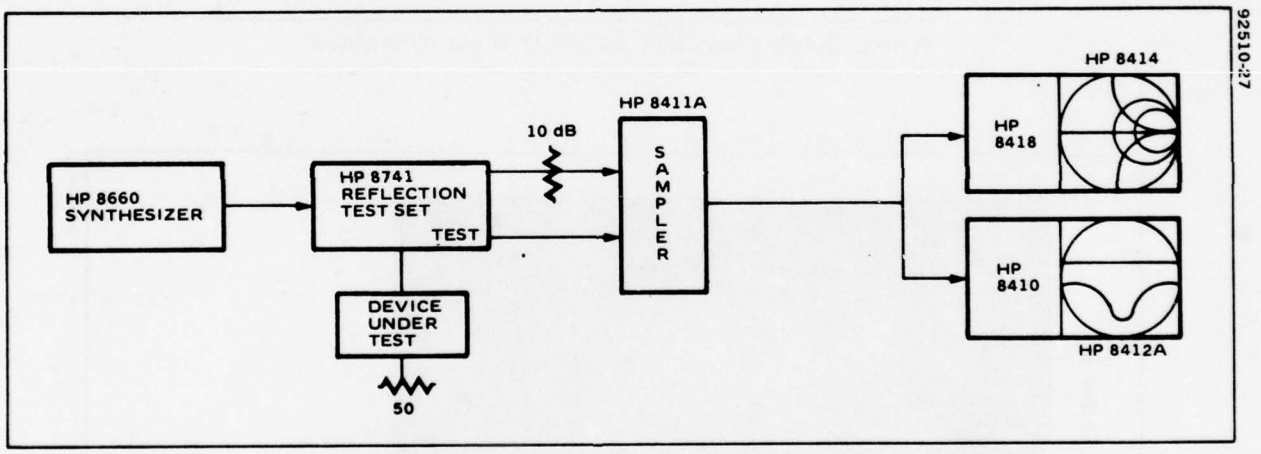
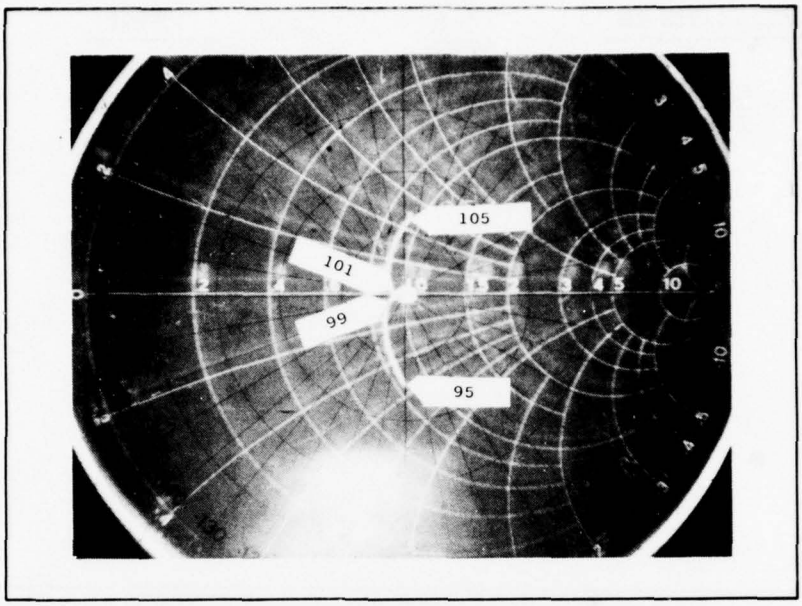
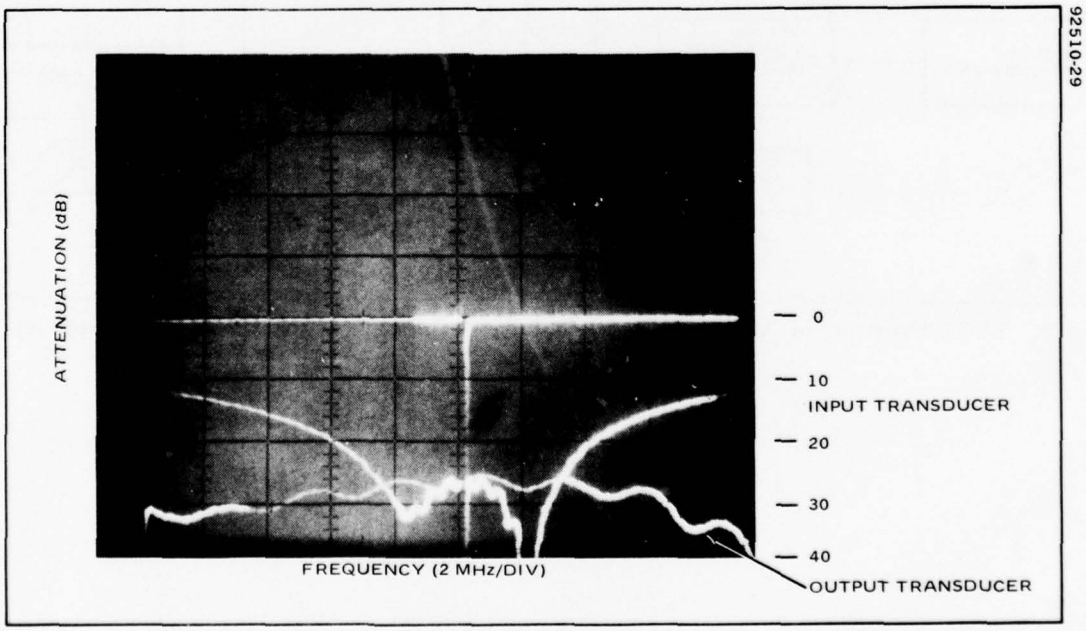


Figure 8. Block Diagram for Measurement of Voltage Standing Wave Ratio in the Frequency Domain



Typical Smith Chart Plot for BP-Q Input Transducer

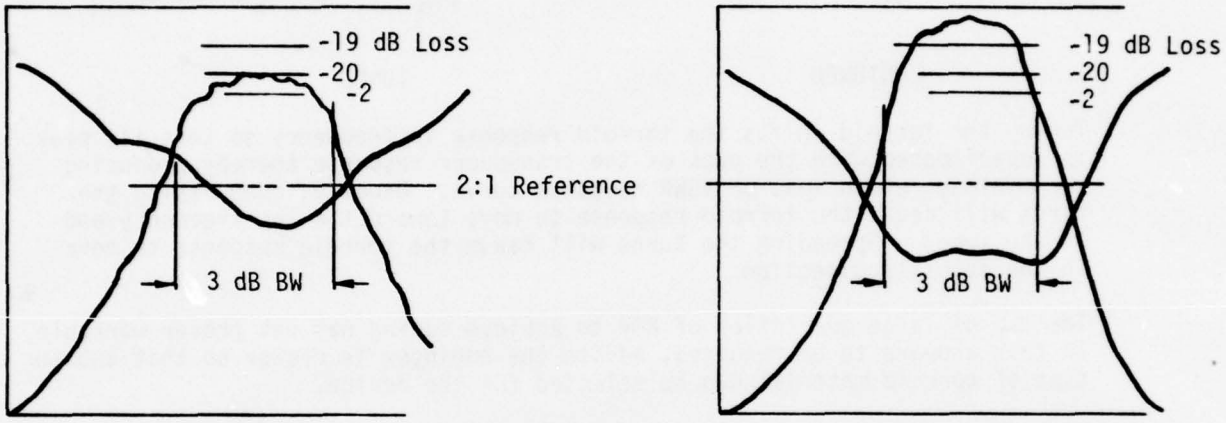


Typical Return Loss Plot for BP-Q Input and Output Transducers

Figure 9

APPENDIX: Tuning Bandpass Filters and Pulse Compression Filters (applies to all types of test equipment setups)

The center frequency of SAW devices is determined by the transducer design and is fixed by the metalized pattern deposited on the surface of the crystal. Tuning the packaged devices does not significantly alter the center frequency although it may skew the response curve and effect the 3dB bandwidth. The major purpose for tuning a SAW device is to minimize the input and output VSWR or "match" the SAW device to external circuit element. A device is "matched" or tuned when the return loss is minimized within the 3dB bandwidth unless otherwise specified. The sketches below illustrate a matched and an unmatched filter response.



UNMATCHED VSWR = 2:1 MIN MATCHED

Thus, tuning is usually done by monitoring the return loss. Tuning is electrically accomplished by the addition of series or parallel inductance to compensate for the inherent capacitance of the metalized pattern. It is physically accomplished by expanding or compressing turns on a torroidal powdered iron core using a pair of tweezers. When the desired response is achieved, the core and the turns on it are held in position by the addition of RTV compound. The RTV compound if used to excess will also influence the tuning. So also will the orientation of the core and the proximity of a metal cover.

The procedure then is to install the unit to be tuned into a properly calibrated test setup and expand or compress the turns on the core whose terminals are connected to the SWR Bridge so that the VSWR response is centered on the 3dB bandwidth of the device.

If the sweep width of the generator is set very wide compared to the bandpass of the device to be tested, it will be noted that the VSWR response is a composite of two curves. One curve is the resonance of the transducer. This is usually approximately equal to the 3dB bandwidth of the device being tested. The second curve is the response of the torroid and its parasitic

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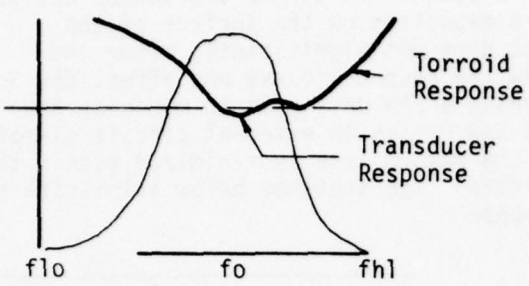
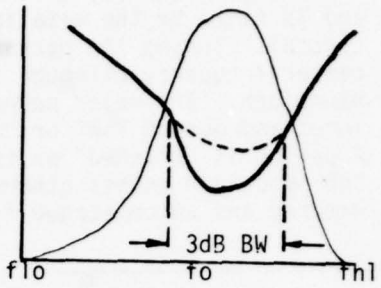
capacitance. This is usually quite broad. The illustration below shows this phenomena.



UNTUNED

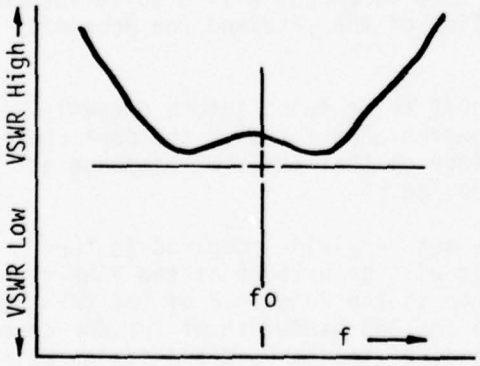


TUNED

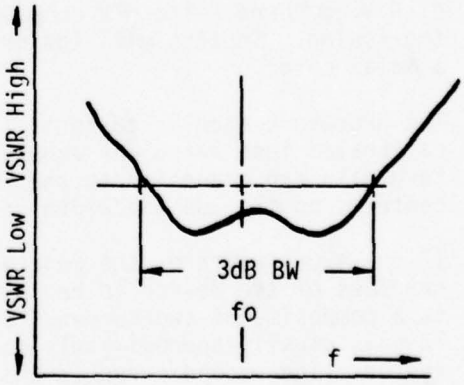
Tuning the torroid shifts the torroid response in frequency so that its peak is superimposed with the peak of the transducer response thereby producing the minimum return loss or VSWR response curve. Usually, compressing the turns will cause the torroid response to move toward the low frequency end of the sweep. Spreading the turns will cause the torroid response to move in the opposite direction.

The use of large quantities of RTV to achieve tuning has not proven workable. If this appears to be required, advise the engineer in charge so that another type of torroid material can be selected for the device.

Most transducers have small metal resistors as a part of their structure. Usually the proper value of resistance in series with the transducer has been established at the design level, however, it may be discovered in tuning that additional resistance is required to properly match the device. This can be caused by variation of metal thickness in fabrication. The indication that more resistance is required occurs when the VSWR response curve is properly tuned frequencywise (both responses superimposed) but the VSWR is too great over the 3dB bandwidth. The illustration below shows the incorrect and correct display.



INSUFFICIENT RESISTANCE



CORRECT RESISTANCE

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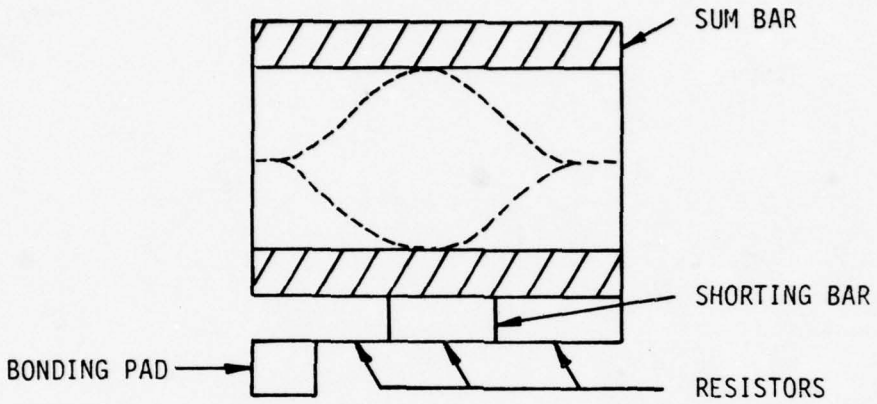
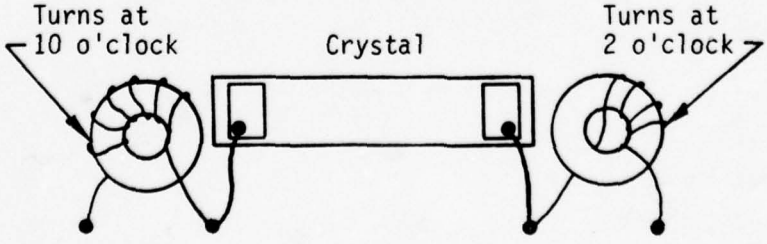
The incorrect condition above can be remedied by the addition of a section of resistance in the transducer, however, a slight detuning may be noted as the resistor will add a small amount of series inductance. This additional inductance can usually be tuned out by spreading the turns on the torroid.

Each transducer has several sections of resistors which are shorted out by thin metal shorts. Resistance is added by scribing through the shorting bars. This is a delicate operation. Consult your supervisor for approval and technique before attemption to add resistance. The sketch below shows a typical transducer pattern with resistors.



The addition of resistors will also increase insertion loss and can be used for this purpose. In general the VSWR will be improved by adding resistance so that increasing insertion loss by this method results in a better VSWR. On the other hand improving VSWR by this method may increase insertion loss beyond specification. In any case advise your supervisors if the addition of resistance is required so he can establish the reason for it and can modify metal thickness or whatever may be the cause.

The orientation of the turns on the torroidal cores sometimes influences feedthrough suppression. In those cases where this has appeared as a problem it has been found that the greatest feedthrough suppression occurs when the turns are positioned away from the crystal as shown below:



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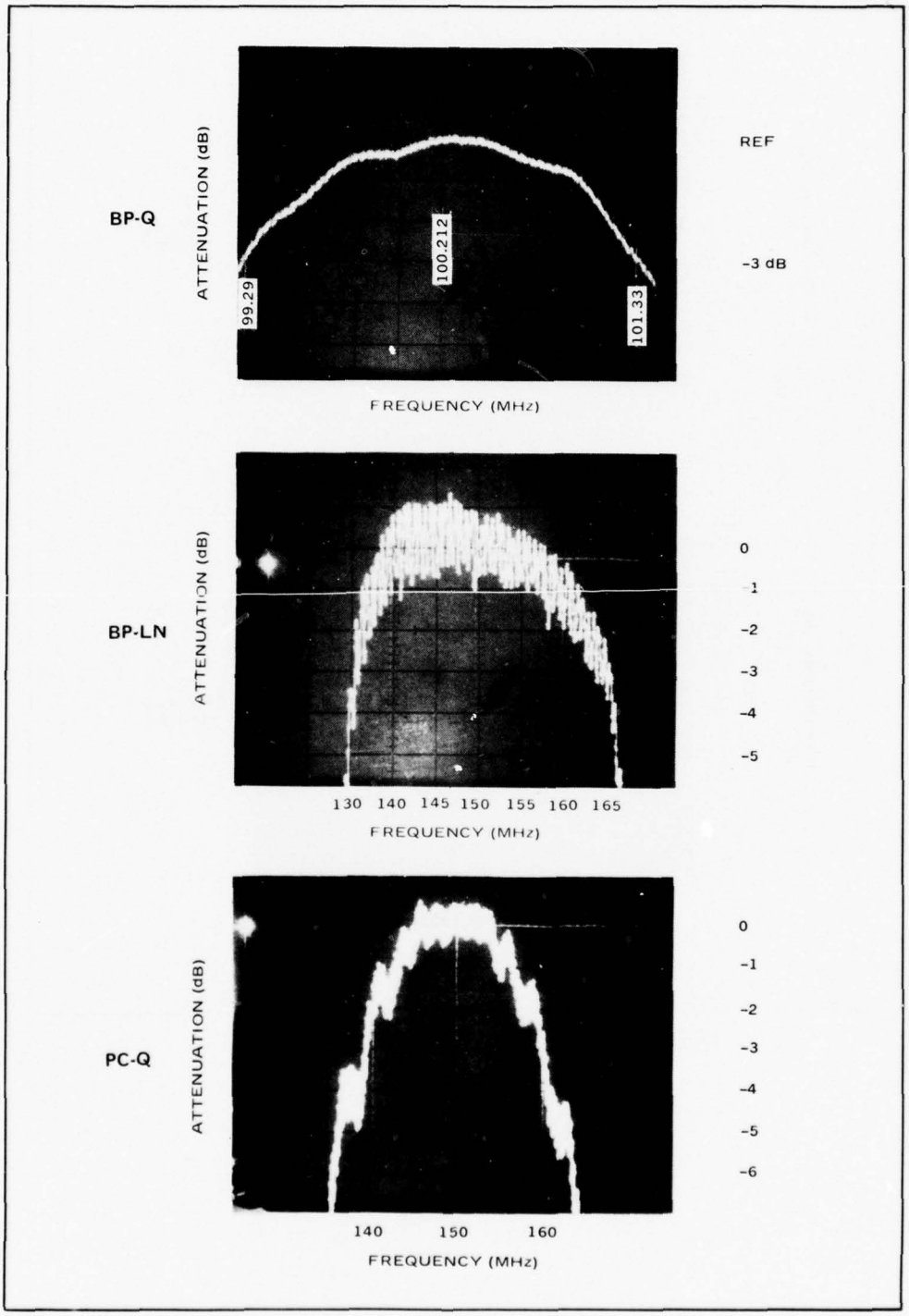
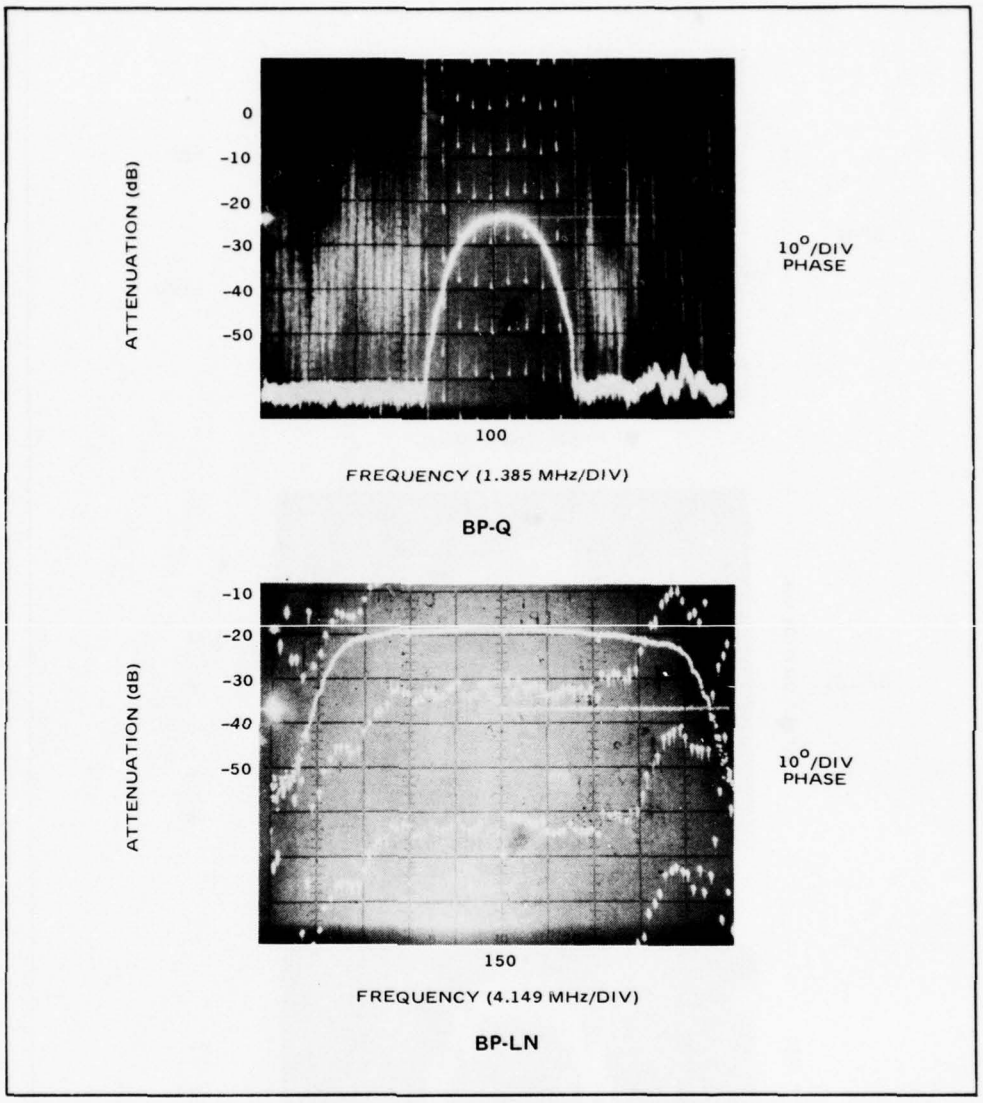
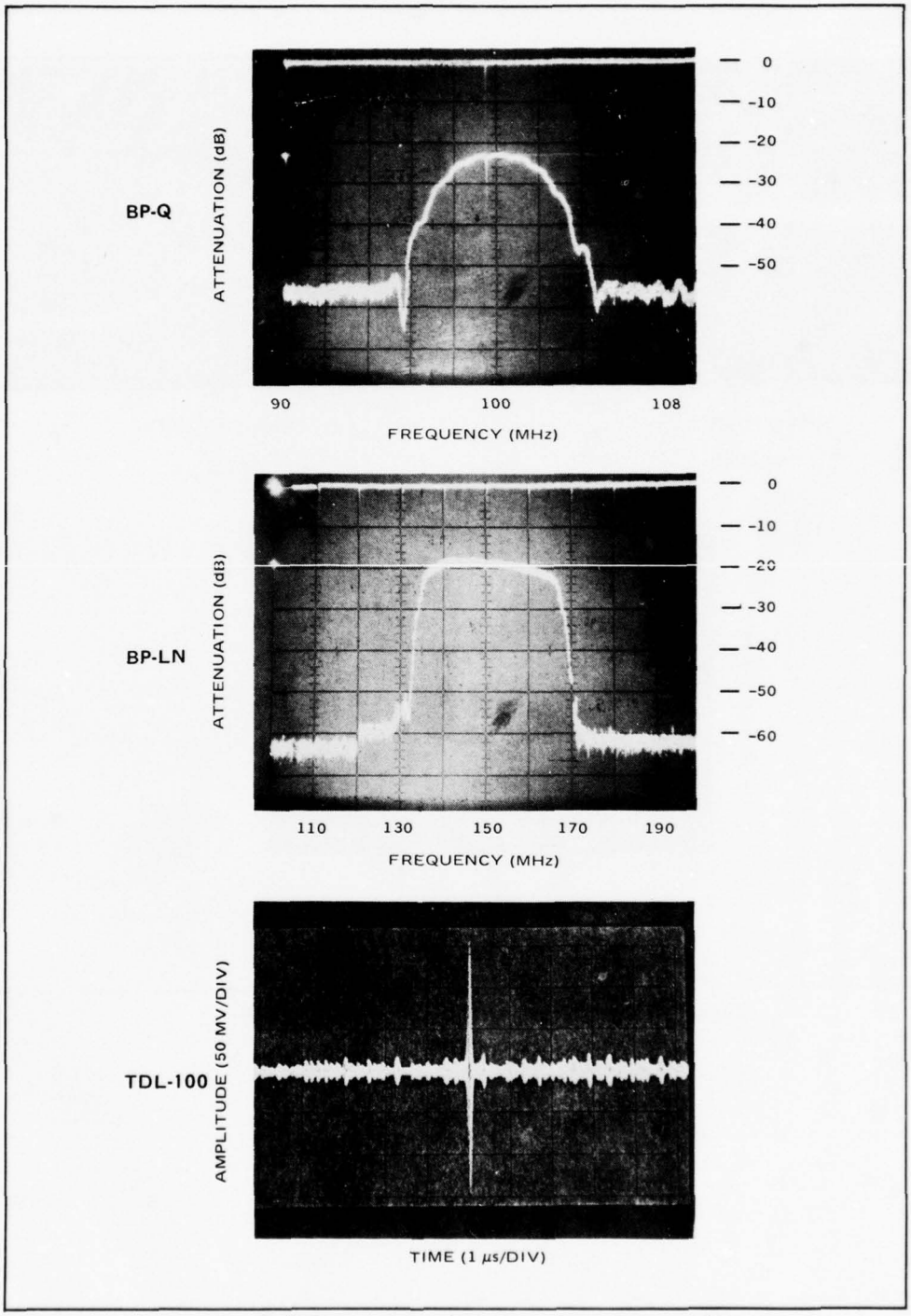
APPENDIX VIII
TYPICAL RAW DATA
FOR MEASUREMENTS
DESCRIBED IN SECTION 3.1.0
FOR APPENDIX VII



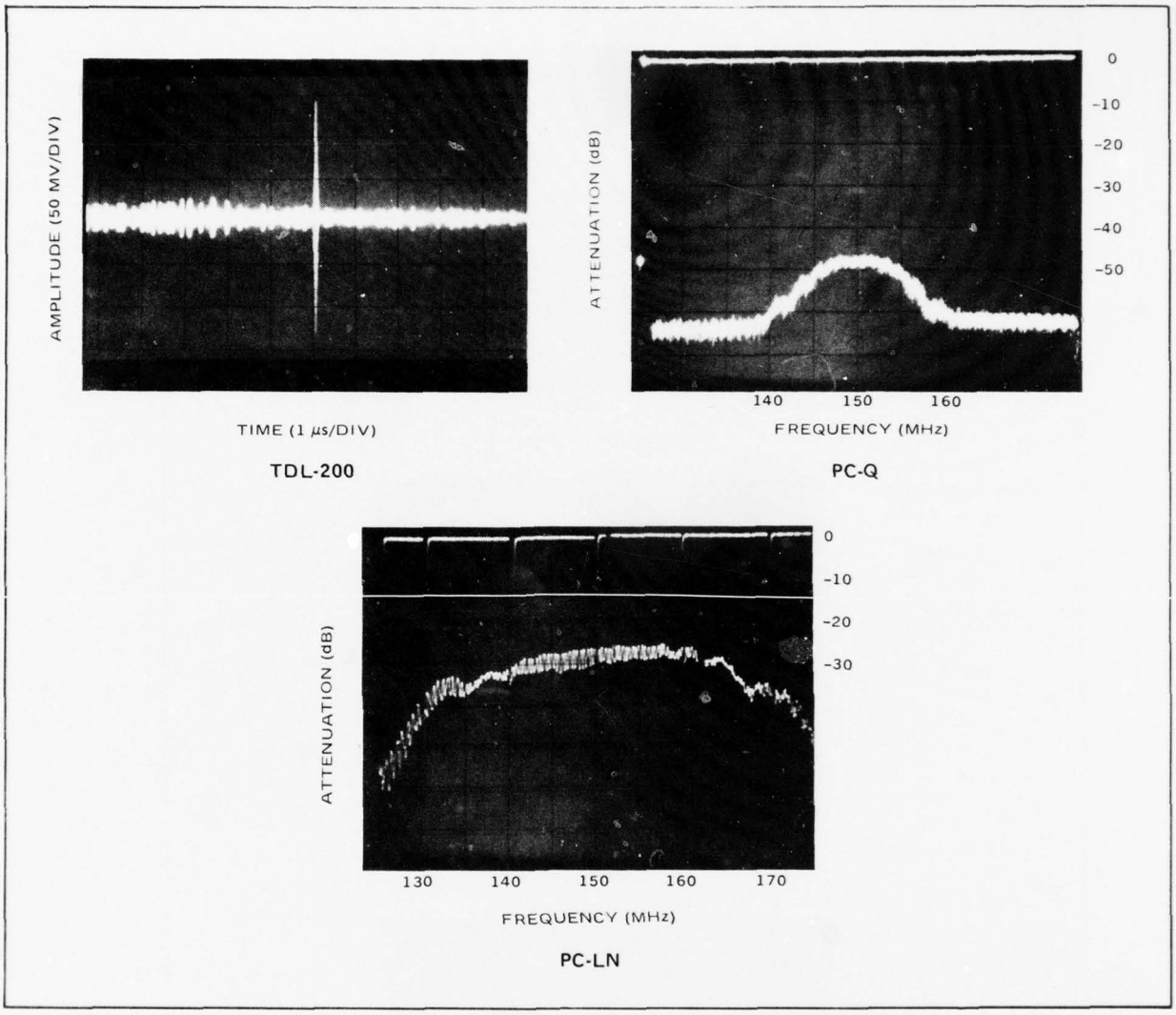
Typical Data: SCS 476 Para 3.10.1 – f_o (MHz); SCS 476 Para 3.10.2 – β -3 dB (MHz)



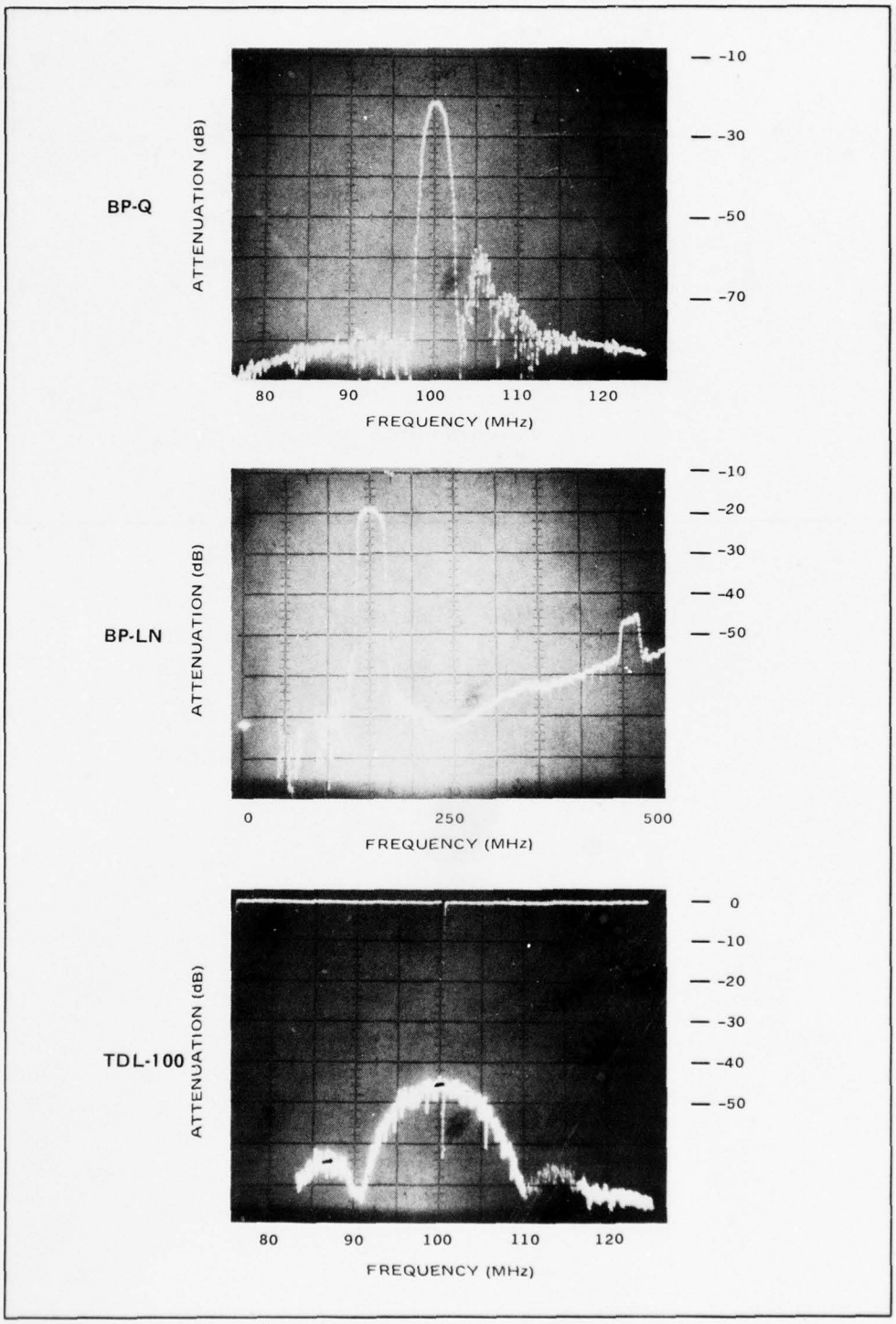
Typical Data: SCS 476 Para 3.10.3 τ (μsec)



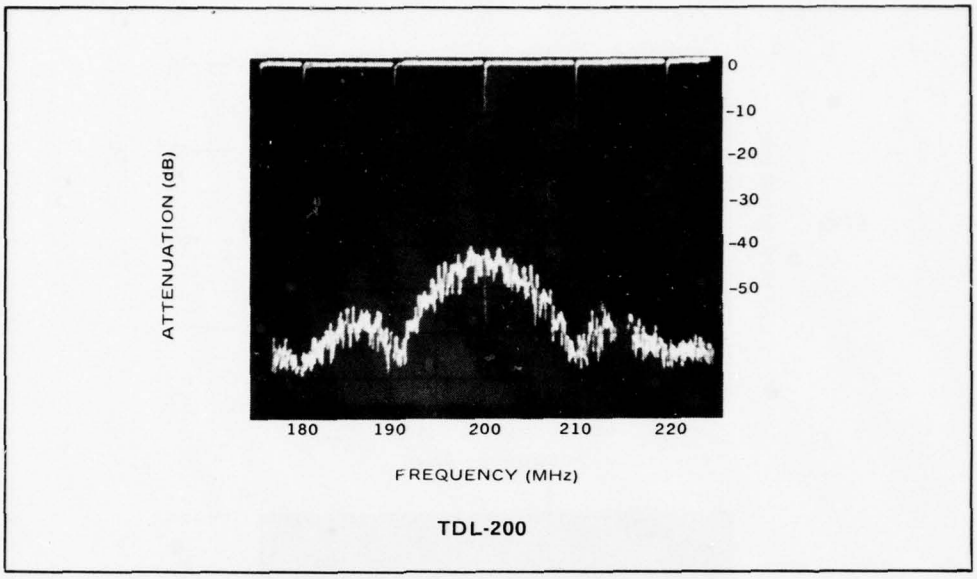
Typical Data: SCS 476 Para 3.10.5 L_{ins} (dB)



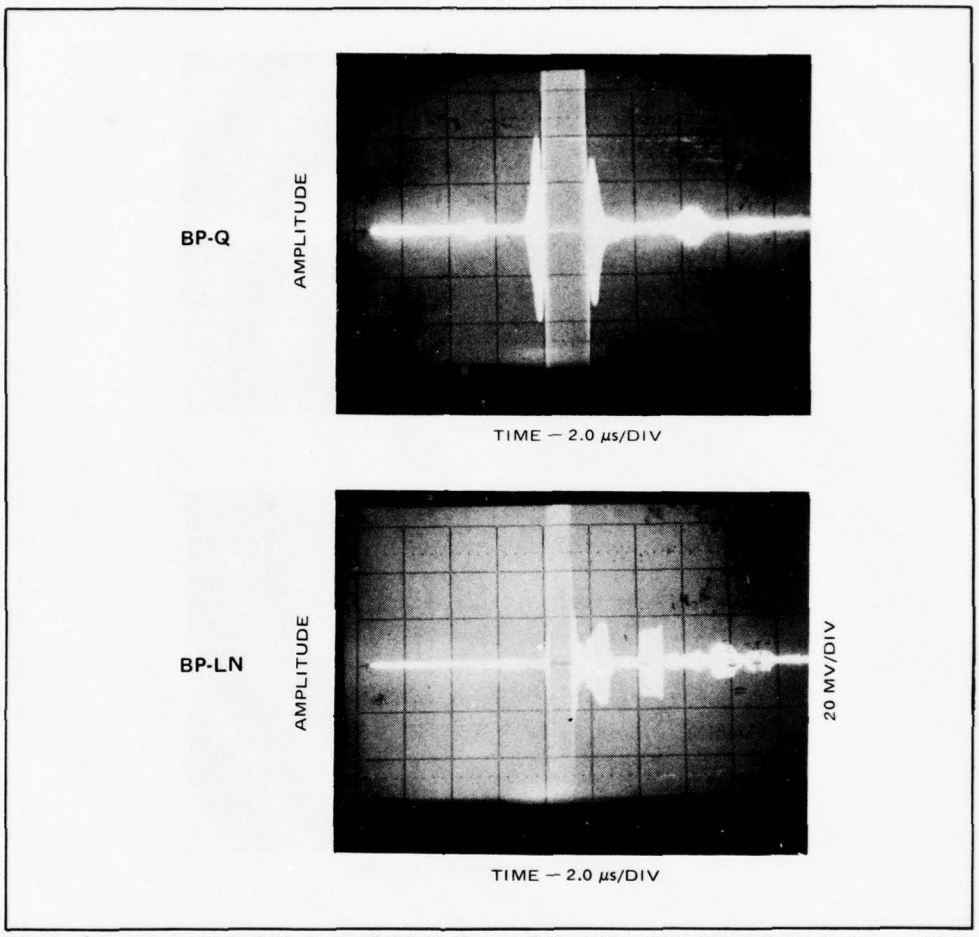
Typical Data: SCS 476 Para 3.10.5 L_{ins} (dB)



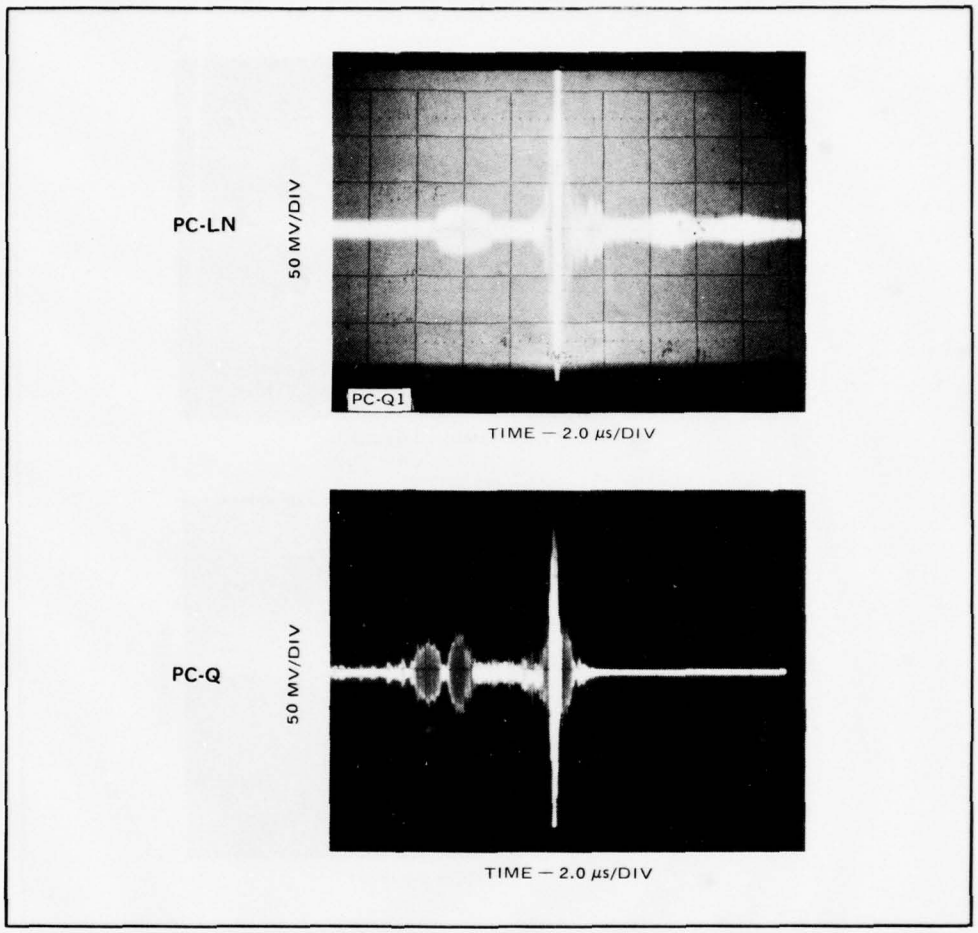
Typical Data: SCS 476 Para 3.10.6 $S_{s.l.}$ (dB)



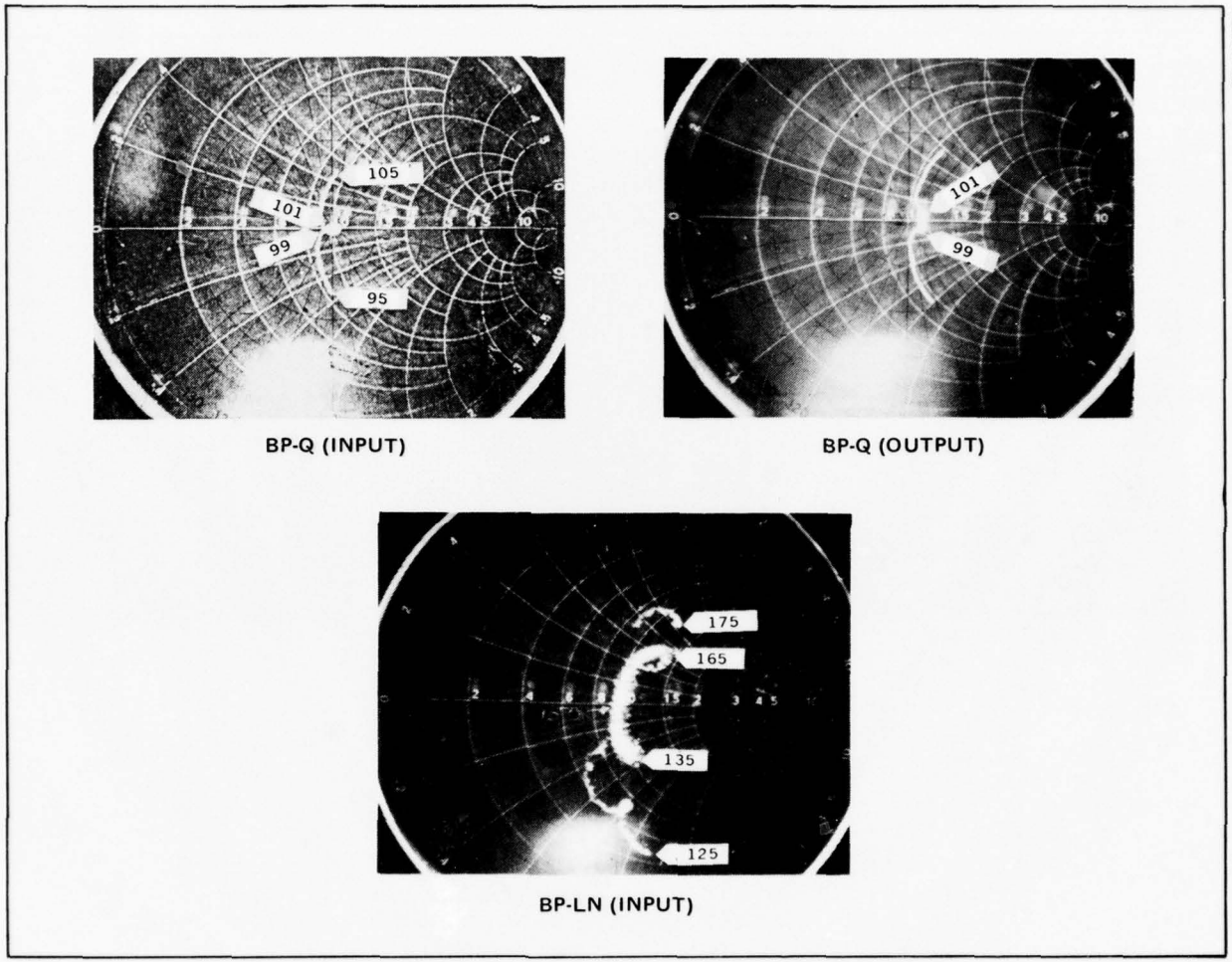
Typical Data: SCS 476 Para 3.10.6 $S_{s.l.}$ (dB)



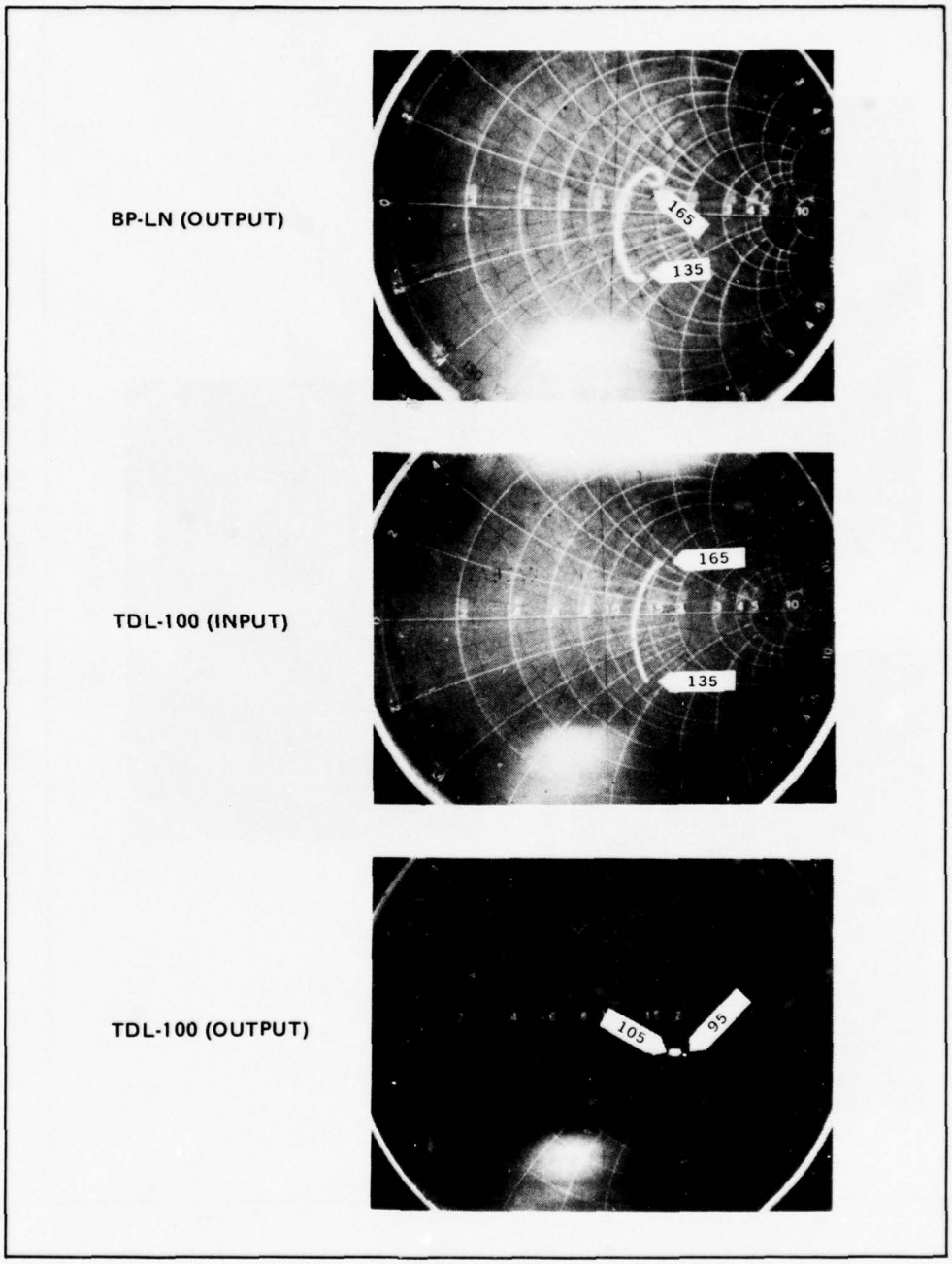
Typical Data: SCS 476 Para 3.10.7 $S_{f.t.}$ (dB); SCS 476 Para 3.10.8 S_{spur} (dB)



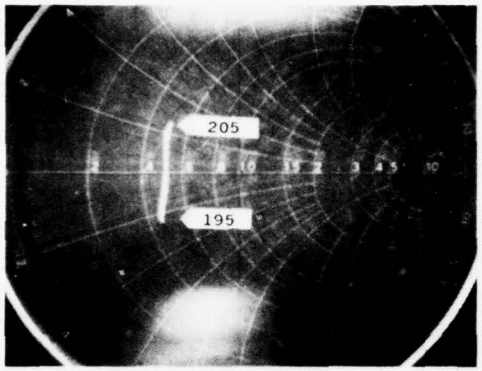
Typical Data: SCS 476 Para 3.10.6 $S_{s.l.}$ (dB); SCS 476 Para 3.10.7 $S_{f.t.}$ (dB); SCS 476 Para 3.10.8 S_{spur} (dB)



Typical Data: SCS 476 Para 3.10.9 VSWR

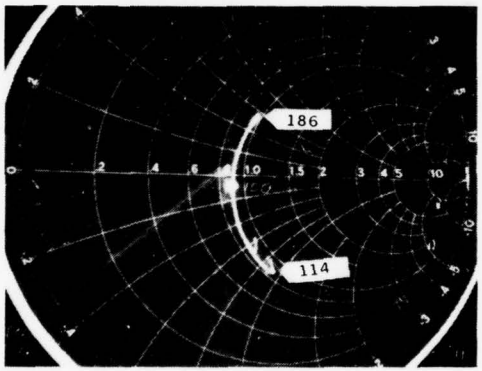


Typical Data: SCS 476 Para 3.10.9 VSWR



TDL-200 (INPUT)

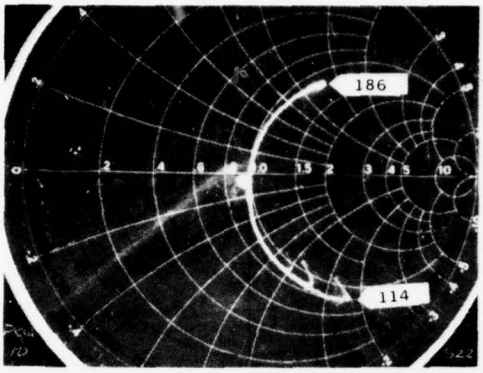
TDL-200 (OUTPUT)



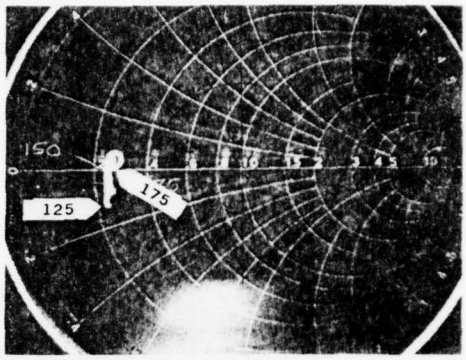
PC-Q (INPUT)

92510-40

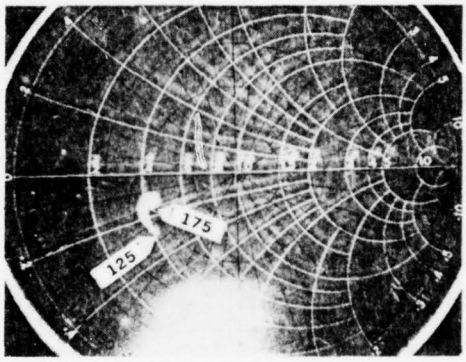
Typical Data: SCS 476 Para 3.10.9 VSWR



PC-Q (OUTPUT)



PC-LN (INPUT)



PC-LN (OUTPUT)

9251041

Typical Data: SCS 476 Para 3.10.9 VSWR

APPENDIX IX

REVISED SPECIFICATION INCORPORATING THE ERRATA SHEET OF APPENDIX I, VOL. 2 AND MODIFICATIONS RESULTING FROM PHASE I REDESIGN

ELECTRONICS COMMAND
TECHNICAL REQUIREMENTS

SCS-476

PHOTOLITHOGRAPHICALLY PRODUCED ACOUSTIC SURFACE WAVE PULSE COMPRESSION, BAND-PASS AND PHASE-CODED FILTERS

1. SCOPE

1.1 Scope. This specification covers the requirements for photolithographic and batch fabrication techniques necessary for the low-cost production of acoustic, surface-wave pulse compression, band-pass, and phase-coded filters.

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-C-39012	Connector, Coaxial, Radio Frequency, General Specification For.

STANDARDS

MILITARY

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes.
MIL-STD-130	Identification Marking of US Military Property.
MIL-STD-202	Test Methods for Electronic and Electrical Component Parts.
MIL-STD-883	Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both title and identifying number or symbol should be stipulated when requesting copies.)

HAC DWG No.
1950512-600
REV. A SHEET 2

3. REQUIREMENTS

3.1 General Description. The filters shall be photolithographically fabricated on lithium niobate or ST quartz substrates.

3.2 Processing.

3.2.1 Metallization. An aluminum film shall be deposited on the piezoelectric substrates using high vacuum or radio frequency sputtering systems. The resistivity shall be less than 2.5 ohms per square.

3.2.1.1 Uniformity of metallization. The absolute thickness of the aluminum film may vary between 300 and 2000 angstrom (A^{o}); the uniformity of the thickness shall be controlled to $\pm$ 5 percent.

3.2.1.2 Adhesion of metallic film. The adhesion of the aluminum film to the substrate shall remain intact on the surface of the substrate (see 4.6.2).

3.2.2 Photoresist application. Photoresist shall be applied to the lithium niobate and ST quartz substrates resulting in a thin uniform coating capable of resolving 2 micron lines.

3.2.3 Photolithographic processing. Contact printing (etching), "lift-off" or "wet contact" printing techniques shall be used, whereby photomasks are applied over the photoresist.

3.2.4 Visual inspection.

3.2.4.1 Wafer. Circuits on the undiced wafer shall be checked using an approved prototype comparison standard to check the sameness of each circuit pattern using a minimum 250X magnification. A minimum of one circuit per wafer or substrate should be examined. A comparison standard is a wafer whose devices meet the specified design and have passed all the electrical tests. This comparison standard will be used as a reference model in order to cull devices with obvious defects in the geometry.

3.2.4.2 Filter package (device). The circuit chip shall be examined after placement in package (without cover) for broken wire bonds, dirt, scratches or other circuit imperfections under 20X magnification.

3.2.5 Dicing of wafer into circuit chips. When required to separate the multiple identical circuits fabricated on the same wafer, a diamond-tipped precision cutting tool shall be used.

3.2.6 Wire bonding. Wire bonding techniques shall be performed so that reliable electrical connections between the surface acoustic wave circuit and the package connectors are made.

3.2.7 Device packaging. Packaging and sealing techniques shall be used so that the resultant hermetically sealed filters shall be capable of meeting all the environmental requirements as specified herein.

3.3 Classes of devices. The required filter type devices are identified as follows:

Devices	Substrate Materials	Center Frequency
a. Linear FM Pulse Compression Filter	ST Quartz	150 MHz
	Lithium Niobate	150 MHz
b. Linear Phase Band-Pass Filter	ST Quartz	100 MHz
	Lithium Niobate	150 MHz
c. Biphase-Coded Tapped Delay Line Filter	ST Quartz	100 MHz
	ST Quartz	200 MHz

3.3.1 Linear FM pulse compression filters. In-line configuration shall be used with internal weighting for sidelobe suppression. Conjugate matched filter pairs shall be fabricated from each substrate material and used to demonstrate pulse compression in each case.

3.3.2 Linear-phase band-pass filters. Multistrip couplers shall be used on lithium niobate to couple the two apodized transducers which effect the weighted filter response.

3.3.3 Biphase-coded tapped delay line filters. Phase-coded tapped delay line filters with center frequencies of 100 and 200 MHz shall use uniform aperture for the phase-coded array. Conjugate matched filter pairs shall be fabricated and used to demonstrate autocorrelation.

3.4 Number of circuit chips per wafer.

3.4.1 Linear-FM pulse compression filters.

3.4.1.1 ST quartz. At least 10 circuit chips shall be fabricated on a single piezoelectric wafer.

3.4.1.2 Lithium niobate. At least 10 circuit chips shall be fabricated on a single piezoelectric wafer.

3.4.2 Linear-phase band-pass filters.

3.4.2.1 ST quartz. At least 15 circuit chips shall be fabricated on a single piezoelectric wafer.

3.4.2.2 Lithium niobate. At least 15 circuit chips shall be fabricated on a single piezoelectric wafer

3.4.3 Biphase-coded tapped delay line filters.

3.4.3.1 At least 7 circuit chips shall be fabricated on a single piezoelectric ST quartz wafer.

3.5 Construction.

3.5.1 Connections (external). The basic filter shall employ two or three parts, depending on the type of filter device with connectors or strip leads. (The precise location should be finalized prior to the confirmatory sample phase.)

3.5.1.1 Connectors. When connectors are used with these filter devices, they shall be series SMA and shall conform to the requirements of MIL-C-39012.

3.5.1.2 Strip leads (lead integrity). When strip leads are used, they shall show no physical or mechanical damage when tested (see 4.6.4.2).

3.5.2 Connections (internal), wire bonding (lead integrity). Gold wire connections of two mil diameter and minimum length, shall show no evidence of loosening or rupturing from the wire bond connection (see 4.6.4.1).

3.5.3 Dimensions. The crystal and package size shall meet the maximum dimensions in inches specified in Table I (see 4.6.3).

Table I. Dimensions.

Classes of Devices	Substrate Material	Max. Circuit Chip Size Substrate (Inches) L W T	Max. Filter Package Size (Inches) L W T
Linear-FM Pulse Type Compression Filters	ST Quartz Lithium Niobate	1.00 x 0.200 x 0.050	2.0 x 1.0 x 0.50
Linear Phase Band Pass Filters	ST Quartz Lithium Niobate	1.00 x 0.200 x 0.050	2.0 x 1.0 x 0.50
Biphase-coded Tapped Delay Lines	ST Quartz (100 MHz) ST Quartz (200 MHz)	2.20 x 0.200 x 0.050 2.2 x 0.200 x 0.050	3.0 x 1.0 x 0.50 3.0 x 1.0 x 0.50

3.6 Hermetic seal. Each filter shall be back-filled with an inert gas and shall show no evidence of leakage (see 4.6.5).

3.7 Thermal shock. Each filter shall show no evidence of mechanical or physical damage and shall exhibit no short circuits (see 4.6.6).

3.8 Solderability (strip leads) (when applicable). Strip leads shall be solderable (see 4.6.7).

3.9 Short circuit and open circuit tests. All chips and filter circuit devices, as applicable, shall be checked for no shorted circuits. A continuity check shall be made to determine that no open circuits exist between the external connection and the surface wave circuit (see 4.6.8).

3.10 Electrical characteristics. Filters shall meet the electrical characteristics and tolerances as specified (see 4.6.9).

3.10.1 Center frequency of operation.

3.10.1.1 Linear FM pulse compression filters.

a. ST Quartz: 150 MHz ± 3 MHz.
b. Lithium Niobate: 150 MHz ± 3 MHz.

3.10.1.2 Linear-phase band-pass filters.

a. ST Quartz: 100 MHz ± 2 MHz.
b. Lithium Niobate: 150 MHz ± 3 MHz.

3.10.1.3 Biphase-coded tapped delay line filters.

a. ST Quartz: 100 MHz ± 2 MHz.
b. ST Quartz: 200 MHz ± 4 MHz.

3.10.2 Bandwidth (3db).

3.10.2.1 Linear FM pulse compression filters.

a. ST Quartz: 50 MHz ± 1 MHz.
b. Lithium Niobate: 50 MHz ± 1 MHz.

This is the difference between the maximum and minimum instantaneous frequencies of the unweighted linear FM waveform to which the characteristics of the respective linear FM pulse compression filters are to be matched.

3.10.2.2 Linear-phase band-pass filters.

a. ST Quartz: 2 MHz ± 0.04 MHz.
b. Lithium Niobate: 30 MHz ± 0.6 MHz.

3.10.2.3 Biphase-coded tapped delay line filters.

a. ST Quartz: 10 MHz ± 0.2 MHz (100 MHz) center frequency.
b. ST Quartz: 10 MHz ± 0.2 MHz (200 MHz) center frequency.

This is the chip rate of the biphase-coded waveforms to which the respective biphase-coded tapped delay line filters are to be matched.

3.10.3 Time-delay.

3.10.3.1 Linear FM pulse compression filters (dispersive delay).

a. ST Quartz: 2 microsec ± 0.02 microsec.
b. Lithium Niobate: 2 microsec ± 0.01 microsec.

3.10.3.2 Linear-phase band-pass filters (nondispersive delay).

a. ST Quartz: 2 microsec ± 0.01 microsec.
b. Lithium Niobate: 2 microsec ± 0.01 microsec.

3.10.3.3 Biphase-coded tapped delay line filters.

a. ST Quartz: 12.7 microsec (100 MHz center frequency
b. ST Quartz: 12.7 microsec (200 MHz center frequency

3.10.4 Time-bandwidth product.

3.10.4.1 Linear FM pulse compression filters.

a. ST Quartz: 100:1
b. Lithium Niobate: 100:1

3.10.4.2 Linear-phase band-pass filters.

a. ST Quartz: 4:1
b. Lithium Niobate: 60:1

3.10.4.3 Biphase-coded tapped delay line filters.

a. ST Quartz: 127:1 (100 MHz center frequency).
b. ST Quartz: 127:1 (200 MHz center frequency).

3.10.5 Insertion loss. (Insertion loss is to be measured by CW)

3.10.5.1 Linear FM pulse compression filters.

a. ST Quartz: 50db ± 5db.
b. Lithium Niobate: 30db ± 3db.

3.10.5.2 Linear-phase band-pass filters.

a. ST Quartz: 20db ± 2db.
b. Lithium Niobate: 20db ± 1.5db.

3.10.5.3 Biphase-coded tapped delay line filters.

a. ST Quartz: 27db ± 3db (100 MHz) center frequency.
b. ST Quartz: 26db ± 3db (200 MHz) center frequency.

To be measured as follows: The matched biphase-coded waveform is generated using a similar tapped delay line with the time-reversed code polarity sequence. The waveform amplitude is limited using saturated amplifiers and then compressed in the tapped delay line filter under test. The insertion loss is the ratio of the input waveform amplitude to the amplitude of the correlation peak of the compressed pulse, expressed in decibels.

3.10.6 Time-sidelobe suppression. S_{sl}

3.10.6.1 Pulse compression filters.

a. ST Quartz: ≥ 25db.
b. Lithium Niobate: ≥ 20db for first sidelobe pair.
≥ 25db for all other sidelobes.

3.10.6.2 Linear-phase band-pass filters.

a. ST Quartz: ≥ 35db.
b. Lithium Niobate: ≥ 35db.

This specified sidelobe is actually the suppression of the insertion loss spectrum, out of band, measured relative to the center frequency level.

3.10.6.3 Biphase-coded tapped delay line filters.

a. ST Quartz: ≥ 17db (100 MHz carrier center frequency).
b. ST Quartz: ≥ 17db (200 MHz carrier center frequency).

3.10.7 Feedthrough suppression. The feedthrough suppression shall be greater than -50db for all types of filters. This shall be relative to the output signal level.

3.10.8 Spurious echo suppression S_{spur} the spurious echo suppression shall be greater than -35db for all types of filters. Spurious echo refers to the double and triple transit phenomena.

3.10.9 Voltage standing wave ratio. Voltage standing wave ratio (VSWR) shall be referenced to a 50 ohm impedance.

3.10.9.1 Pulse compression filters.

a. ST Quartz: ≤ 2.5:1.
b. Lithium Niobate: ≤ 3.5:1.

3.10.9.2 Linear-phase band-pass filters.

a. ST Quartz: ≤ 2:1.
b. Lithium Niobate: ≤ 3:1.

3.10.9.3 Biphase-Coded tapped delay line filters.

a. ST Quartz (100 MHz carrier frequency) ≤ 4:1.
b. ST Quartz (200 MHz carrier frequency) ≤ 3:1.

Over the operating band with a 50 ohm impedance (ZO).

3.11 High temperature storage. Filters shall show no evidence of physical or mechanical damage and no electrical short circuits after subjection to a temperature of 75°C (see 4.6.10 and 4.6.8).

3.12 Shock (specified pulse). Filters shall show no evidence of mechanical or physical damage and no electrical short circuits (see 4.6.11 and 4.6.8).

3.13 Vibration (low frequency). Filters shall show no evidence of mechanical or physical damage and no electrical short circuits (see 4.6.12 and 4.6.8).

3.14 Moisture resistance. Filters shall show no evidence of mechanical or physical damage and no short circuits. All of the electrical characteristics (final) shall be met in accordance with the limits provided in the government approved contractor's plan (see 4.6.13 and 4.6.8).

3.15 Life. After 500 hours of life, the filters shall show no evidence of mechanical or physical damage; and shall meet all of the electrical characteristics (final) in accordance with the limits provided in the government approved contractor's plan (see 4.6.14).

3.16 Marking. All markings shall remain legible throughout processing and testing in accordance with MIL-STD-130.

3.16.1 Wafer. Identification shall be provided on each chip on the substrate to indicate the manufacturer; crystal type; batch or lot; crystal cut and orientation.

3.16.2 Filter. Identification of the type of device along with a descriptive identifying number indicating operating frequency and bandwidth.

3.17 Workmanship. Chips and filters shall be processed in such a manner as to be uniform in quality and shall be free from cracks or other defects that will affect life, serviceability and appearance.

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection. The contractor is responsible for the performance of all inspections specified herein. The contractor may utilize his own facilities or any commercial laboratory acceptable to the government. Tests shall be performed under the supervision of a government representative. Inspection records of the examinations and tests shall be kept complete and available to the government as specified in the contract.

4.2 Classification of inspection. Inspection shall be classified as follows:

a. First article inspection (does not include preparation for delivery) (see 4.4).
b. Quality conformance inspection.

4.3 Inspection condition. Unless otherwise specified herein, all inspections shall be in accordance with the test conditions specified in general requirement of MIL-STD-202.

4.4 First article inspections. This inspection shall consist of all the tests in tables III and IV including the use of the contractor submitted government-approved plan on test methods and procedures for determining the electrical characteristics and the electrical characterisitcs final limits. No failures in excess of those indicated shall be permitted.

4.4.1 Sample.

4.4.1.1 Wafers. (See table II.)

4.4.1.2 Circuit chips. The wafers shall be diced into discrete circuit chips with the exclusion of one wafer for each type of substrate and shall be submitted for inspection as indicated in table II.

4.4.2 Test routine.

4.4.2.1 Wafer submission. Sample units shall be subjected to the inspection specified in table III, in the order shown prior to dicing into discrete circuit devices. Ten (10) each of the first four categories in table II shall be tested and seven (7) each of the last two categories (ST Quartz 100 and 200 MHz, respectively). There shall be no failures.

4.4.2.2 Circuit devices. Eighty-four (84) operable filter circuit devices shall be submitted to the inspections specified in table IV, in the order shown. Twelve sample units shall be used for group II inspection only. The remaining units shall be subjected to group I inspection and subdivided into the remaining groups for their particular examination or test. Forty-two sample units of each substrate material (100 MHZ and 200 MHZ) of the operable biphase-coded tapped delay line filter circuit devices shall be submitted to the inspections specified in Table IV, in the order shown, using 36 sample units for group I; 6 sample units for group II; 9 sample units for groups III and IV; 6 sample units for group V, and 12 sample units for group VI. The number of defects shall remain as indicated for each group excluding group VI, where only 1 defect shall be allowed.

Table II. Class of devices with minimum number of wafers, circuits per wafer and total number of operable filter circuit devices.

Class of devices	Minimum Nr. of wafers	Minimum Nr. of circuits per wafer	Operable filter circuit devices
Linear FM pulse compression filters	10-ST Quartz	10	84
	10-Lithium Niobate	10	84
Linear band-pass filters	10-ST Quartz	15	84
	10-Lithium Niobate	15	84
Biphase-coded tapped delay line filters	7-ST Quartz (freq 100 MHz)	7	42 } 84
	7-ST Quartz (freq 200 MHz)	7	42 }

Table III. First article inspection of each type of wafer.

Examination or test	Requirement paragraph	Test paragraph
Marking	3.16.1	
Visual check (using a standard for reference under magnification) (250X)	3.2.4.1 3.17	4.6.1.1
Adhesion of metallic film	3.2.1.2	4.6.2
Short circuit	3.9	4.6.8

Table IV. First article inspection of each class of filter devices (circuit devices).

Examination or test	Requirement paragraph	Test paragraph	Number of Samples		Number of Defects	
			All Others	TDL	All Others	TDL
Group I						
Visual check (20X magnification)	3.2.4.2 3.17	4.6.1.2				
Marking	3.16.2					
Dimensions	3.5.3	4.6.3	72	36	0	0
Strip lead (lead integrity)	3.5.1.2	4.6.4.2				
Internal wire bonding (lead integrity)	3.5.2	4.6.4.1				
Electrical characteristics	3.10	4.6.9				
Group II						
Solderability (when applicable)	3.8	4.6.7	12	6	0	0
Group III						
High temperature storage	3.11	4.6.10				
Electrical characteristics	3.10	4.6.9				
Center frequency	3.10.1 thru 3.10.1.3, incl.		18	9	0	0
Insertion loss	3.10.5 thru 3.10.5.3, incl.					
Group IV						
Life	3.15	4.6.14				
Short circuit test	3.9	4.6.8	18	9	1	1
Electrical characteristics (Final)	3.10	4.6.9				
Group V						
Hermetic seal	3.6	4.6.5	12	6	0	0
Short circuit test	3.9	4.6.8				
Group VI						
Vibration	3.13	4.6.12				
Short circuit test	3.9	4.6.8				
Shock	3.12	4.6.11				
Short circuit test	3.9	4.6.8				
Thermal shock (10 cycles)	3.7	4.6.6	24	12	2	1
Short circuit test	3.9	4.6.8				
Moisture resistance	3.14	4.6.13				
Short circuit test	3.9	4.6.8				
Electrical characteristics (Final)	3.10	4.6.9				

4.4.3 Defectives.

4.4.3.1 Wafers. No defects shall be allowed in table III; any defects shall be cause for refusal to grant first article inspection approval.

4.4.3.2 Filter circuit devices. Defects in excess of those allowed in table IV shall be cause for refusal to grant first article inspection approval.

4.5 Quality conformance inspection.

4.5.1 Inspection of product for delivery. Inspection of products for delivery shall consist of groups A, B and C inspection.

4.5.1.1 Inspection lot. An inspection lot shall be as specified in MIL-STD-105 and applies to each of the six types of wafers or filter circuit devices, as applicable.

4.5.1.2 Group A inspection. Group A inspection shall consist of the examinations and tests in table V in the order shown. Subgroup I examination and tests are on wafers and subgroup II on the filter circuit devices.

Table V. Group A inspection.

Examination or test	Requirement paragraph	Method paragraph
Subgroup I		
Marking	3.16.1	
Adhesion of metallic film	3.2.1.2	4.6.2
Short circuit	3.9	4.6.8
Visual Inspection	3.2.4.1, 3.17	4.6.1
Subgroup II		
Visual (magnification 20X)	3.2.4.2, 3.17	4.6.1.2
Marking	3.16.2	
Hermetic seal	3.6	4.6.5
Strip lead (lead integrity)	3.5.1.2	4.6.4.2
Internal wire bonding (lead integrity)	3.5.2	4.6.4.1

4.5.1.2.1 Sampling plan. 100 percent inspection shall be performed on subgroup I on the wafers which shall then be diced into discrete circuits; and subgroup II inspection shall be performed using 100 percent inspection.

4.5.1.2.2 Rejected samples. If during the 100 percent inspection of subgroup I, screening indicated that over 30 percent of the total filter circuit devices on all wafers (undiced) be discarded, the lot (wafers) shall be rejected.

4.5.1.3 Group B Inspection. Group B inspection shall consist of the tests specified in table VI, in the order shown and shall be made on sample units which have been subjected to and have passed group A, subgroup II inspection.

Table VI. Group B inspection.

Examination or test	Requirement paragraph	Method paragraph
Eletrical characteristics		
Center frequency of operation	3.10.1, 3.10.1.1, 3.10.1.2, 3.10.1.3	4.6.9
Bandwidth	3.10.2, 3.10.2.1, 3.10.2.2, 3.10.2.3	4.6.9
Time delay	3.10.3, 3.10.3.1, 3.10.3.2, 3.10.3.3	4.6.9
Time-bandwidth product	3.10.4, 3.10.4.1, 3.10.4.2, 3.10.4.3	4.6.9
Insertion loss	3.10.5, 3.10.5.1, 3.10.5.2, 3.10.5.3	4.6.9
Time-sidelobe suppression level	3.10.6, 3.10.6.1, 3.10.6.2, 3.10.6.3	4.6.9
Feedthrough suppression	3.10.7	4.6.9
Spurious echo suppression	3.10.8	4.6.9
Voltage standing wave ratio (VSWR)	3.10.9	4.6.9

4.5.1.3.1 Sampling plan. Sampling plan shall be in accordance with special procedures for small sample inspection of MIL-STD-105. The AQL shall be 6.5 percent defective using inspection level S-4.

4.5.1.3.2 Test routine. The samples specified in 4.5.1.3 shall be subjected to the tests in table VI in the order shown.

4.5.1.3.3 Rejected lots. If an inspection lot is rejected, the contractor may withdraw the particular lot once, screen out defectives, and reinspect once. Such lots shall be kept separate from new lots and shall be clearly identified as reinspected lots. Rejected lots shall be reinspected using tightened inspection.

4.5.1.3.4 Deleted.

4.5.1.4 Group C inspection. Group C inspection shall consist of the tests specified in table VII, in the order shown. Group C inspection shall be made on sample units selected from inspection lots which have passed groups A and B inspections.

4.5.1.4.1 Sampling plan. Six sample units of each type of filter circuit device shall be selected for each of subgroups 1, 2 and 3 at random from each lot as specified in 4.5.1.1.

4.5.1.4.1.1 Test routine. The samples selected in accordance with 4.5.1.3 shall be subjected to the tests shown in table VII. Not more than one defect shall be allowed for a single group of six samples.

4.5.1.4.2 Disposition of samples. Filter circuit devices subjected to group C inspection shall not be delivered on the contract or order. Samples emanating from lots which have passed groups A and B inspection may be delivered on the contract.

Table VII. Group C inspection.

Examination or test	Requirement paragraph	Test paragraph
Group I		
High temperature storage	3.11	4.6.10
Short circuit	3.9	4.6.8
Hermetic seal	3.6	4.6.5
Short circuit	3.9	4.6.8
Subgroup II		
Solderability (strip leads) (when applicable)	3.8	4.6.7
Life	3.15	4.6.14
Electrical characteristics (final)	3.10	4.6.9
Subgroup III		
Vibration	3.13	4.6.12
Short circuit	3.9	4.6.8
Shock	3.12	4.6.11
Short circuit	3.9	4.6.8
Thermal shock (10 cycles)	3.7	4.6.6
Short circuit	3.9	4.6.8
Moisture resistance	3.14	4.6.13
Electrical characteristics (final)	3.10	4.6.9

4.5.1.4.3 Noncompliance. If a sample fails to pass group C inspection, the contractor shall take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same materials, processes, and so forth, and which are considered subject to the same failure. Acceptance of the product shall be discontinued until corrective action, acceptable to the government, has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspections or the inspection which the original sample failed at the option of the government). Groups A and B inspection may be reinstituted; however, final acceptance shall be withheld until the group C reinspection has shown that the corrective action was successful. In the event of failure, action shall be furnished to the contracting officer.

4.6 Methods of examination and test.

4.6.1 Visual.

4.6.1.1 Wafer (see 3.2.4.1 and 3.17). A government approved prototype comparison standard shall be utilized to check the sameness of each circuit pattern using a minimum of 250X magnification.

4.6.1.2 Filter device (see 3.2.4.2 and 3.17). An examination for circuit inspections shall be performed under 20X magnification.

4.6.2 Adhesion of metallic film (see 3.2.1.2). A one-inch strip of pressure sensitive cellophane tape, conforming to type I, class A of Federal Specification L-T-90, shall be applied to the metallized surface, adhesion side down, employing firm hand pressure. The tape shall then be removed with one abrupt motion, and the adhesive side examined for detached particles of metallic film.

4.6.3 Dimensions (see 3.5.3). Dimensions shall be measured using a micrometer.

4.6.4 Lead integrity (internal wire bonding and strip lead). Filter devices shall be tested in accordance with method 2011 of MIL-STD-883, method 4.6.4.1 or 4.6.4.2 as applicable.

4.6.4.1 Internal wire bonding. The following details shall apply:

a. Test condition D - Tension.
b. Weight to be attached to lead - 2 grams.
c. Length of time weight is to be attached - A minimum of 10 seconds.

4.6.4.1.2 Strip lead. Test condition A - Tension.

4.6.5 Hermetic seal (see 3.6). Filter devices shall be tested in accordance with method 112B, MIL-STD-202. The following details shall apply:

a. Test condition - C.
b. Leak-rate sensitivity - 10^{-8} atm cc/sec.
c. Procedure IV, test for gross leaks using test condition A.

4.6.6 Thermal shock (see 3.7). Filter devices shall be tested in accordance with method 107, MIL-STD-202, test condition A (10 cycles).

4.6.7 Solderability (strip leads only, when applicable) (see 3.8). Filter devices shall be tested in accordance with method 2003 of MIL-STD-883. Each strip lead on a filter device shall be tested.

4.6.8 Short circuit and open circuit tests. All chips and filter circuit devices, as applicable, shall be tested for short circuits by any suitable means including the open circuit test between the external connection and the surface wave circuit.

4.6.9 Electrical characteristics (see 3.10). The government approved contractor's plan of electrical test methods, procedures and limits of degradation (electrical characteristics final) shall be used.

4.6.10 High temperature storage (see 3.11 and 3.9). Filter devices shall be tested in accordance with method 1008 of MIL-STD-883. The following details shall apply.

a. Test condition - A (75°C).
b. Test duration - 72 hours.
c. At the end of the exposure period, the devices shall be allowed to stabilize at room temperature and the filter device tested for short circuits.

4.6.11 Shock (specified pulse). Filter devices shall be tested in accordance with method 213 of MIL-STD-202. The following details shall apply:

a. Test condition - I
b. Method of mounting - Filter devices shall be rigidly mounted by their normal mounting means.

4.6.12 Vibration (low frequency) (see 3.13). Filters shall be tested in accordance with method 201 of MIL-STD-202. The filters shall be rigidly mounted by their normal mounting means.

4.6.13 Moisture resistance (see 3.14). Filters shall be tested in accordance with method 106D of MIL-STD-202. The following details shall apply:

a. Polarizing voltage - 50 Vdc
b. Final measurements - Before measurements, all units shall be removed from the test chamber and stabilized at room temperature. The filters shall be visually inspected and all electrical characteristics shall be performed and degradation limits shall be as indicated in the government approved contractor's plan.

4.6.14 Life (at elevated ambient temperature) (see 3.15). Filters shall be tested in accordance with method 108 in MIL-STD-202. The following details and exceptions shall apply.

a. Mounting - Normal mounting means as used in a system or sub-system.
b. Distance between filter devices - 6 inches.
c. Test temperature and tolerance - $85^{\circ}C \begin{smallmatrix} + 10^{\circ} \\ - 5^{\circ} \end{smallmatrix} C$.
d. Final measurements - Before measurements are made, all units shall be removed from the test chamber and stabilized at room temperature. All electrical characteristics shall be performed and degradation limits shall be as indicated in the government approved contractor's plan.

5. PREPARATION FOR DELIVERY.

The substrates, circuit chips and filters shall be in accordance with best commercial practices.

6. NOTE.

Normally the filter device will be employed as a plug-in device, hence soldering will not normally be required.

HUGHES

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☒ CLASS II ☐ RECORD CORRECTION

CHANGE IDENT NO. 94549

SHEET 1 OF 1

TITLE	PROJECT	ECP/UPN, ETC.	DRAWING NO.	REV.	NO.
DELAY LINE, SURFACE ACOUSTIC WAVE-DESIGN/PERFORMANCE SPECIFICATION	MICROELECTRONICS/SAW		1950512-600	A	

TYPE OF CHANGE: ☒ MANDATORY ☐ MANUFACTURING CONVENIENCE ☐ MANUFACTURING OPTION

	ORG CODE	DATE		ORG CODE	DATE
PREPARED BY: C. CRAIG	12-67-10	79/12/22	APPROVED: J. K. Sanguis	12-67-10	79-12-23
CHECKED BY: [illegible]	12-67-10	79/12/16			
P/L MAINTENANCE					

CONTROL ITEM		CONFIGURATION ITEM	
DRAWING NO.	EFFECTIVITY	DRAWING NO.	EFFECTIVITY
1950512-100			

DISPOSITION OF ITEMS: ☐ ITEMS CONFORM ☐ USE ☐ REWORK AS FOLLOWS: SEE REWORK INSTRUCTIONS

REASON AND DESCRIPTION – SEE BELOW FOR P/L CHANGES

REASON : UPDATE CIRCUIT PERFORMANCE SPECIFICATION.

COMPLETELY REVISED AND REDRAWN.

STANDARD RELEASE

ITEM NO.	LINE NO.	ADD	DELETE	QTY REQ.	UNIT OF MEAS	MFG CODE IDENT NO.	PART OR IDENT NUMBER	DESCRIPTION	SPECIFICATION OR REFERENCE	FROM REF. DESIGNATION	THRU	WEIGHT IN LBS.	P/L NOTE	ZONE

4775 GS 1/77

1X-16

APPENDIX X
THE EFFECT OF SELECTION OF CORE MATERIAL AND COIL PLACEMENT ON DEVICE FEEDTHROUGH AND VSWR

SELECTION OF CORE MATERIAL AND COIL PLACEMENT AND THEIR EFFECT ON FEEDTHROUGH AND VSWR IN SAW BANDPASS FILTERS

Experience gained in Phase II of the MMT Program suggested an empirical investigation of the effect of tuning coil core permeability upon feedthrough suppression and VSWR. Such an experiment was carried on with those values of core permeability which were readily available. The linear phase bandpass filter on quartz (BP-Q) was used as a test vehicle. The problem came to light when it was discovered that bandpass filters and tapped delay lines exhibited marginal feedthrough suppression when tested in the time domain after being tuned for bandpass and VSWR in the frequency domain.

The return loss pattern is the composite response of the transducer return loss response and that of the series tuning inductor. The transducer response is fixed and consists of a minima approximately centered around the 3 dB bandwidth of the filter, while the tuning inductor response is a broader assymetrical dip. The tuning inductor response can be skewed in frequency from below the transducer response to a point above f_o of the filter by compressing or expanding the turns. The optimum point occurs when both minima are superimposed. When there are too few turns on the tuning inductor the curve can be displaced toward the lower frequencies by re-orienting the core, using the inherent shunt parasitic capacitance to ground, or enhancing this shunt capacitance with large amounts of RTV between the core and the package platform. The RTV has a higher dielectric constant and increases the shunt capacitance markedly. The added capacitance, however, transforms the real component of the input impedance and a large value of R must be added in series to match the device, thereby degrading insertion loss. For this reason, the use of shunt capacitance is avoided.

The core material currently in use for BP-Q was powdered iron T-16-6 material by Micrometals with 11 turns of #30 wire. Lower-mu material (T-16-10, T-16-12) and higher-mu (T-16-3) cores were selected, and equivalent number of turns to produce the same inductance put on each core using 35AWG wire. The finer wire makes tuning physically easier with very little difference in inductance value.

Table I shows the type of core material, permeability (μ), quality factor per MHz, (Q/MHz), number of turns of 35 gauge wire to create equivalent inductance, (#T), inductance per 100 turns of wire (L/100T), bandwidth at a VSWR of 2:1, and device feedthrough suppression.

The required 3 dB bandwidth at 2:1 VSWR was 2.0 MHz. For the BP-Q the T-16-10 and T-16-12 cores could be made to exceed this value significantly by the addition of series resistance. Note that the lower-mu (T-16-10 and T-16-12) cores produced the higher feedthrough suppression and were less sensitive to orientation. In general, tuning for VSWR is easiest to accomplish with more turns distributed around the core, while feedthrough is minimized when the turns are tightly compressed and carefully oriented.

TABLE I

Micrometals Core Mat'l Designation	μ	Q/ MHz	No. of Turns 35 GA.	L(μh)/ 100T	Bandwidth (MHz) @ 2:1 VSWR	Feed-thru (dB)	Best Core Orient. o'clock
1. T-16-3	35	–	6	61	–	35	N/A
2. T-16-6	8-1/2	100/25	12	19	2.2	48	2:00
3. T-16-6	8-1/2	100/25	11	19	2.1	50	2:00
4. T-16-10	6	100/25	13	13	1.6	50	1:30
5. T-16-12	4	115/50	18	8	2.1	60	N/A
6. T-16-12	4	115/50	16	8	1.9	55	1:00

The plots of device insertion loss and return loss for the output transducer versus frequency in Figure 1 depict the results of this experiment which are tabulated above. It should be noted that the minimum series resistance value for the input transducer was used. That is, the output series resistors were left as deposited and no scribing of the shorting bars was used. Thus, the results are due entirely to the effects of the toroidal inductor.

By comparing the broadband frequency response, the individual toroid and transducer return loss responses can be deduced. The T-16-3 core shows the very broad inductor response predicted for the use of high-mu core material. However, the return loss response of the transducer is inverted, the desired 2:1 VSWR is not achieved, and the feedthrough is severe. The width of the inductor response for the other materials was seen to narrow as mu is decreased, which is possibly due to lower selfresonant frequencies resulting from the larger number of turns. These trends are depicted by the dashed line on the plots for the T-16-6 material in Figure 1.

This data indicated the following improved electrical test sequence during tuning: the turns are compressed and oriented to 2 o'clock position before tuning the VSWR. Minimum tuning is then used to obtain the 2:1 VSWR and feedthrough is checked immediately thereafter and before package sealing.

Final device toroid configurations used for Phases III and IV can be seen in Table II.

A second experiment was performed on another device type to elucidate the relationship between toroid orientation and feedthrough isolation. The configurations in Figure 2 were fabricated and tested using the same package, crystal and toroids for all configurations. Descriptions of the various test configurations are discussed below:

Test 1 – Hybrid Flatpack Performance (Fig. 2A): The frequency response of a properly grounded package complete with cover was measured. Greater than 90 dB of input to output signal isolation was observed over the filter passband.

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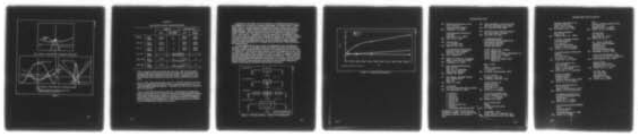

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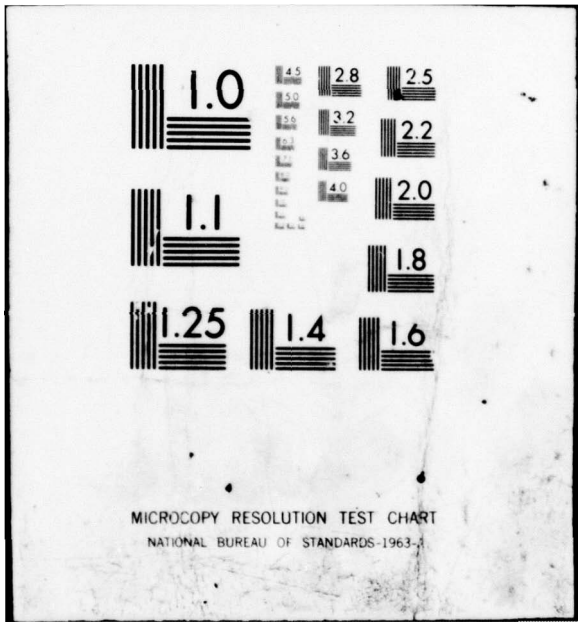
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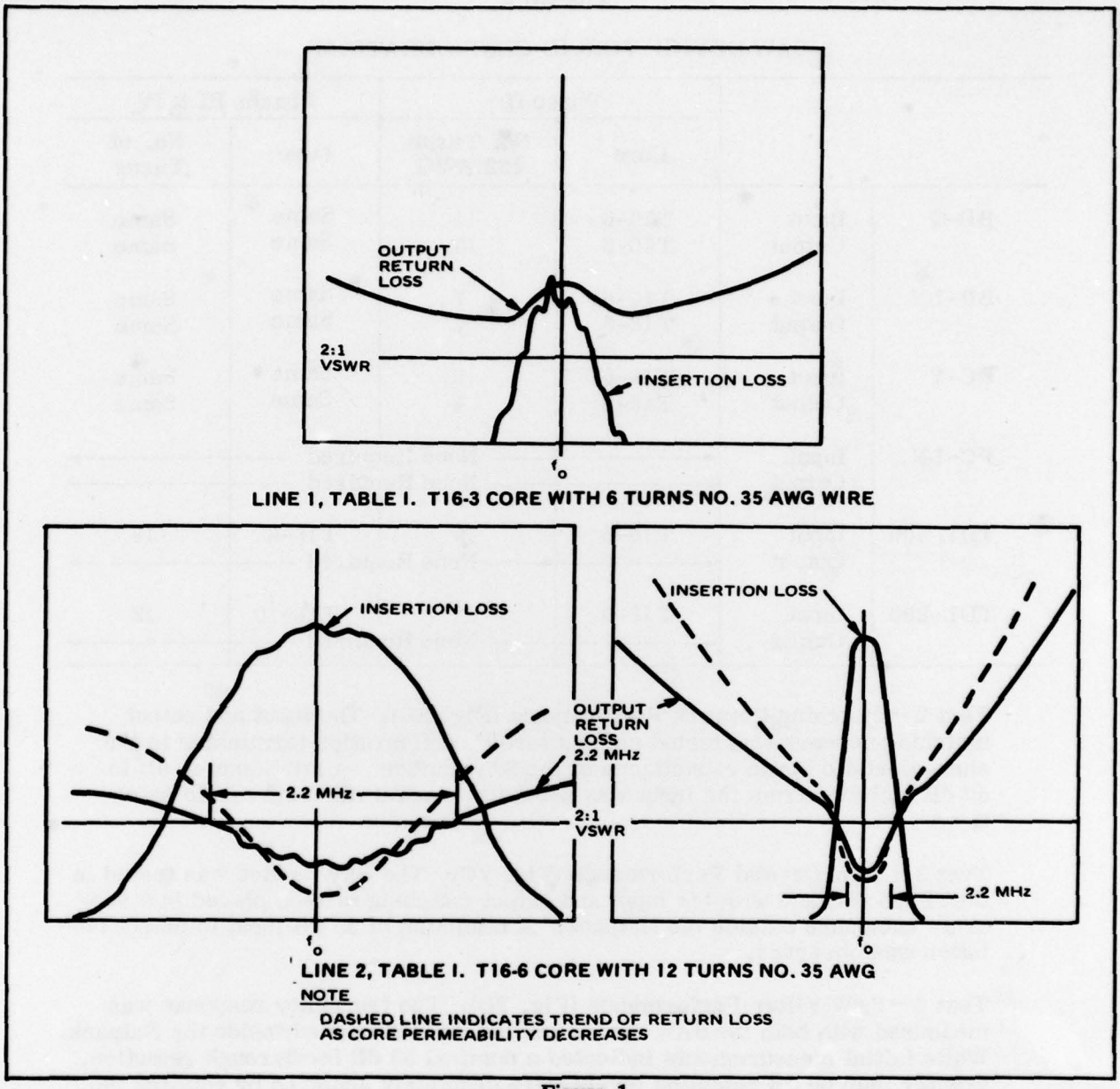
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OUTPUT
RETURN
LOSS
2:1
VSWR
INSERTION LOSS
f_o
LINE 1, TABLE I. T16-3 CORE WITH 6 TURNS NO. 35 AWG WIRE
INSERTION LOSS
2.2 MHz
OUTPUT
RETURN
LOSS
2.2 MHz
2:1
VSWR
INSERTION LOSS
2.2 MHz
f_o
f_o
LINE 2, TABLE I. T16-6 CORE WITH 12 TURNS NO. 35 AWG
NOTE
DASHED LINE INDICATES TREND OF RETURN LOSS
AS CORE PERMEABILITY DECREASES

Figure 1.

TABLE II

SAW DEVICE TOROID CONFIGURATIONS

		Phase II		Phases III & IV	
		Core	No. Turns #32 AWG	Core	No. of Turns
BP-Q	Input	T16-6	11	Same	Same
	Output	T16-6	13	Same	Same
BP-LN	Input	T16-6	7	Same	Same
	Output	T16-6	7	Same	Same
PC-Y	Input	T16-6	6	Same	Same
	Output	T16-6	4	Same	Same
PC-LN	Input	None Required			
	Output	None Required			
TDL-100	Input	T16-6	19	T16-6	18
	Output	None Required			
TDL-200	Input	T16-0	23	T16-10	12
	Output	None Required			

Test 2 – Matching Network Performance (Fig. 2B): The input and output matching network was tested using a toroid configuration terminated in the characteristic static capacitance of the SAW device. A minimum 45 dB to 50 dB isolation from the input was noted for several different toroid selections.

Test 3 – SAW Crystal Performance (Fig. 2C): The SAW device was tested in the above package with the input and output matching toroids placed in a separate enclosure outside the flatpack. A minimum of 35 dB input to output isolation was observed.

Test 4 – SAW Filter Performance (Fig. 2D): The frequency response was measured with both the SAW device and the toroids located inside the flatpack. While initial measurements indicated a nominal 35 dB feedthrough rejection, greater than 60 dB rejection levels were ultimately achieved by rotating the input and output toroid configurations. When spiral inductors were utilized, only 45 dB feedthrough isolation was achieved.

Implications of the effect of toroid orientation on feedthrough suppression are the mandated use of toroids to minimize feedthrough in situations where a septum cannot be used. Certain septum configurations have been noted to have a detrimental effect on package hermeticity yields after sealing on projection and seam welded packages. Also, since the conclusion of this program toroids have been noted to degrade with high temperature storage for temperatures approaching 150°C. See Figure 3. In addition, toroids can detune due to mechanical or thermal stress for certain environments, implying the required use of spiral inductors. In situations which preclude the use of toroids and septums, the only choices remaining to optimize feedthrough are the use of very long time delays (implying large transducer separations) or a package which has the lid in close proximity to the crystal surface.

It would appear that the major source of feedthrough in the semiconductor package is related to an interaction between the SAW transducers for this device, since the isolation achieved with only toroids in the package was 45 to 50 dB (Test 2 – Figure 2B). The fact that planar inductors improved feedthrough by only 10 dB over the bare crystal (Test 4, Figure 2D vs Test 3, Figure 2C) appears to indicate that the toroids interact with the fields over the transducers in a manner such that the input transducer/output transducer interaction is minimized. The fact that the planar spiral inductors offered only 45 dB isolation can be explained by the concentration of fields in close proximity to the spiral for this inductor configuration, thereby minimizing the interaction with the SAW transducers.

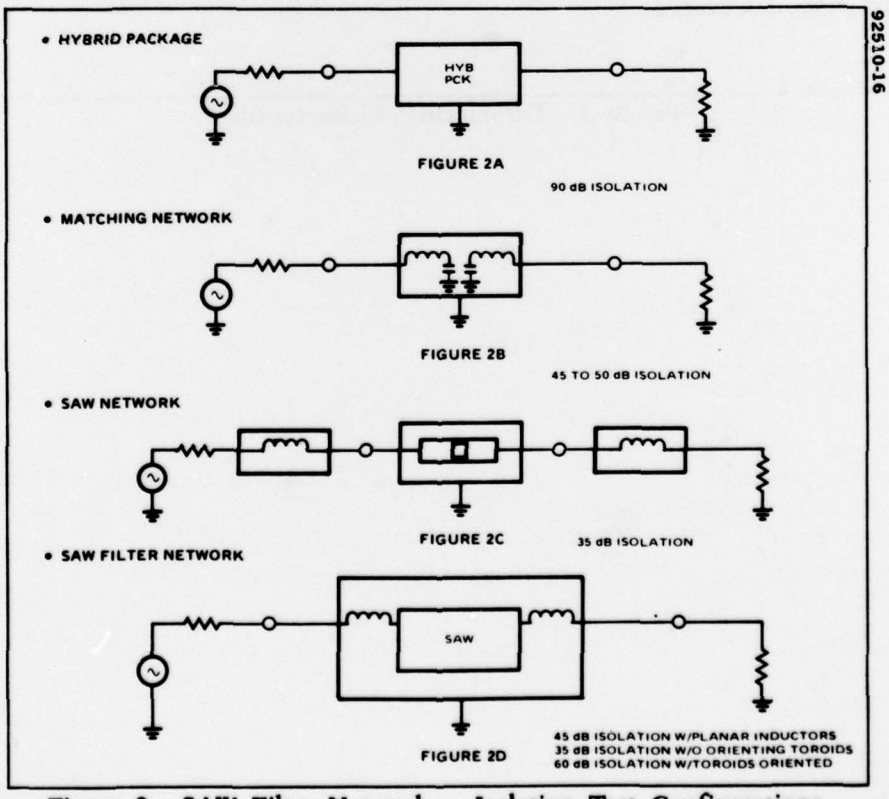

Figure 2. SAW Filter Network – Isolation Test Configurations

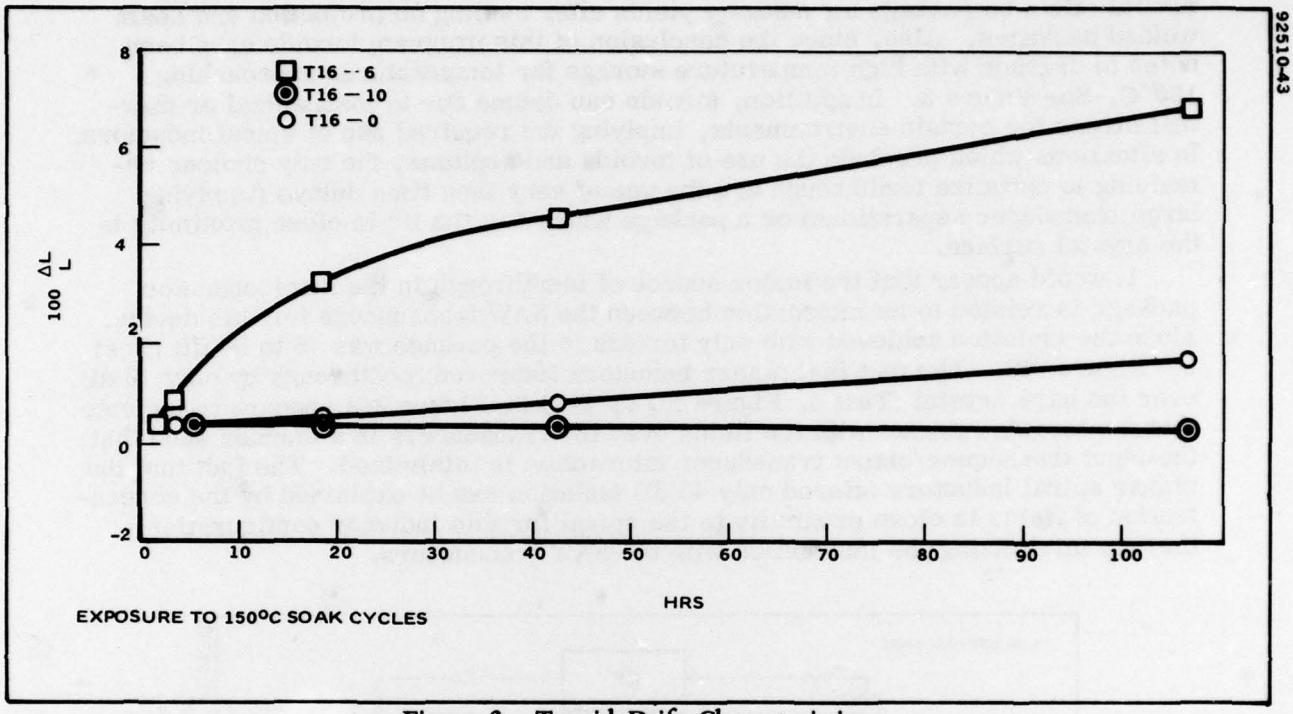

Figure 3. Toroid Drift Characteristics

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